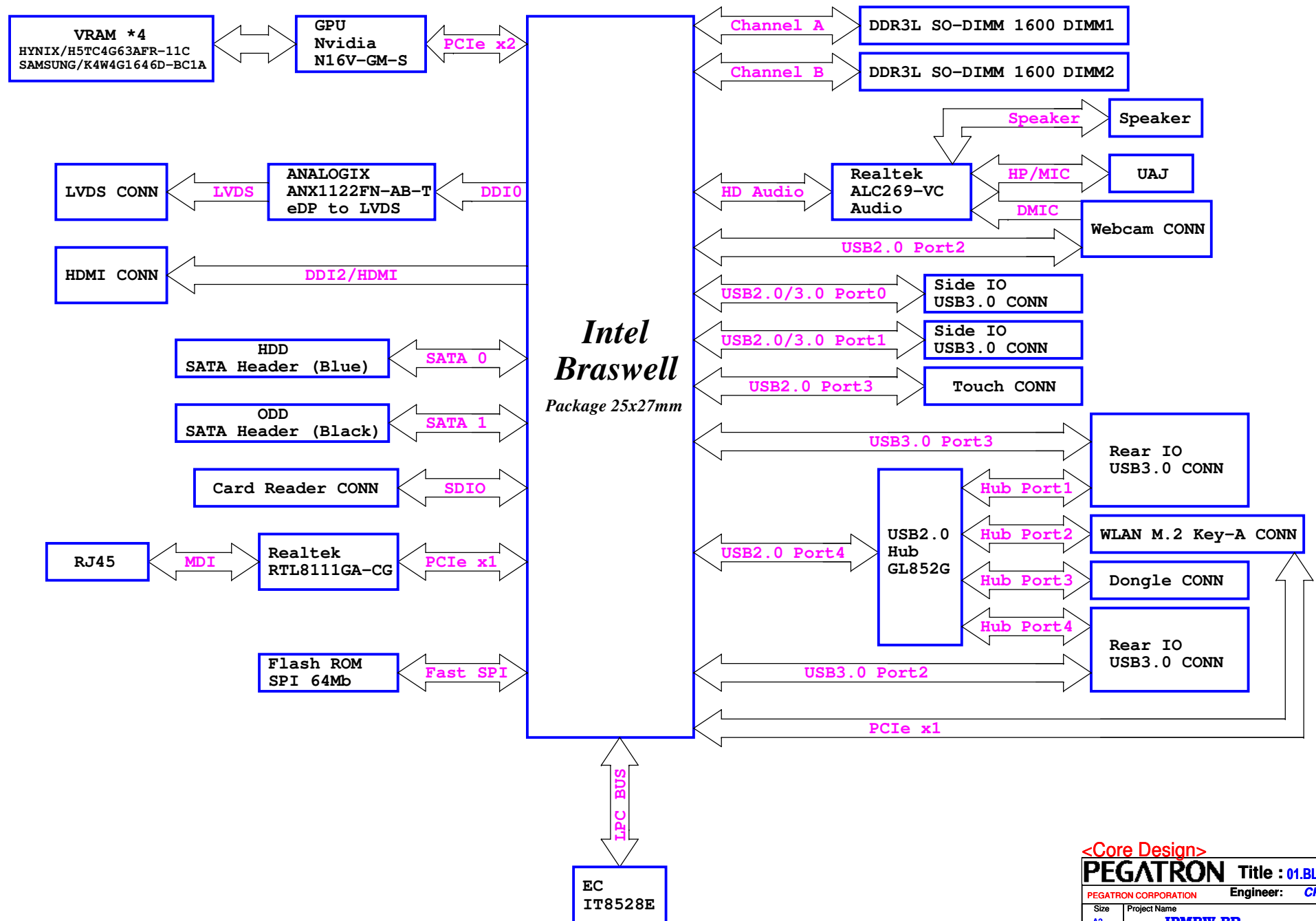


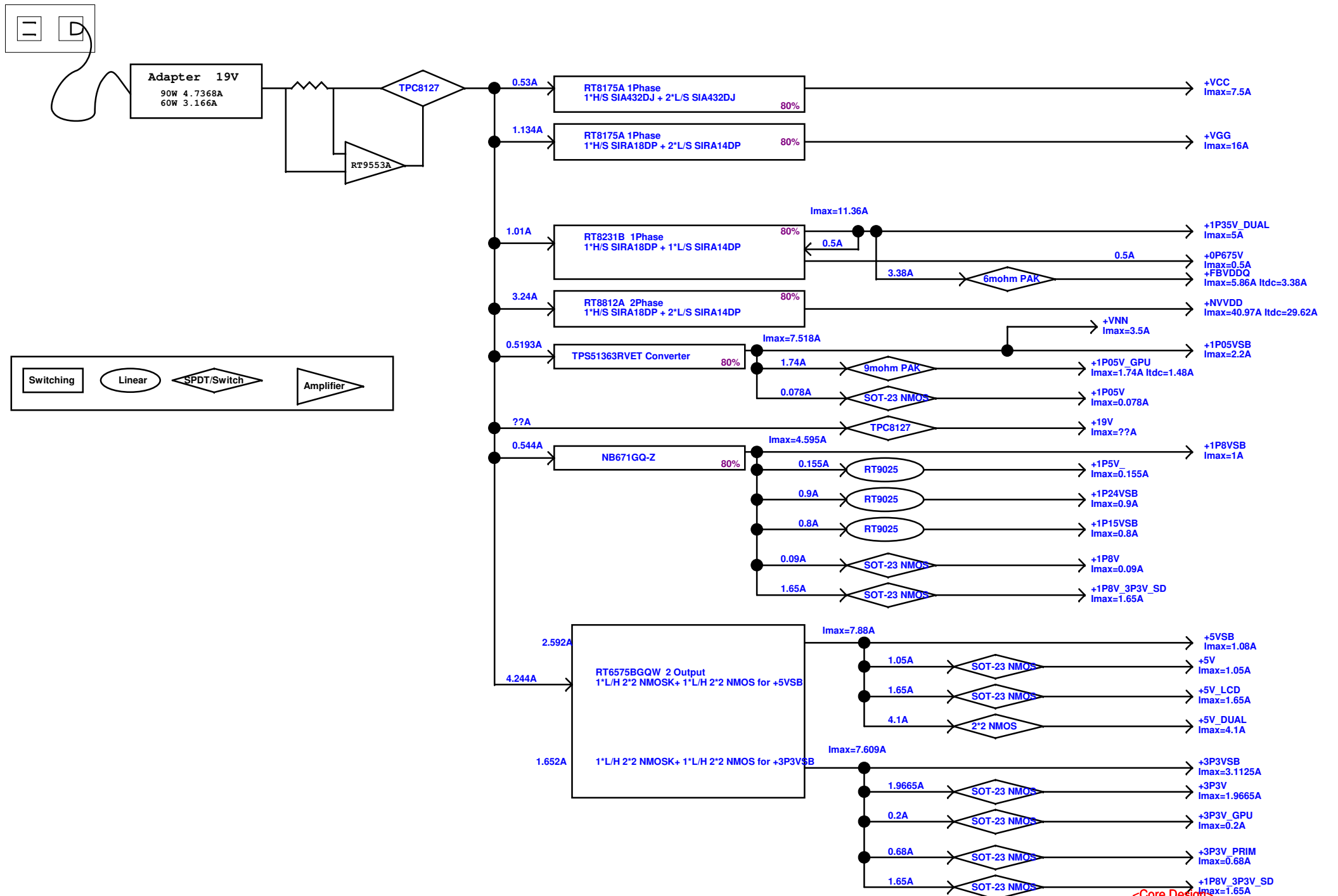
IPMBW-BR

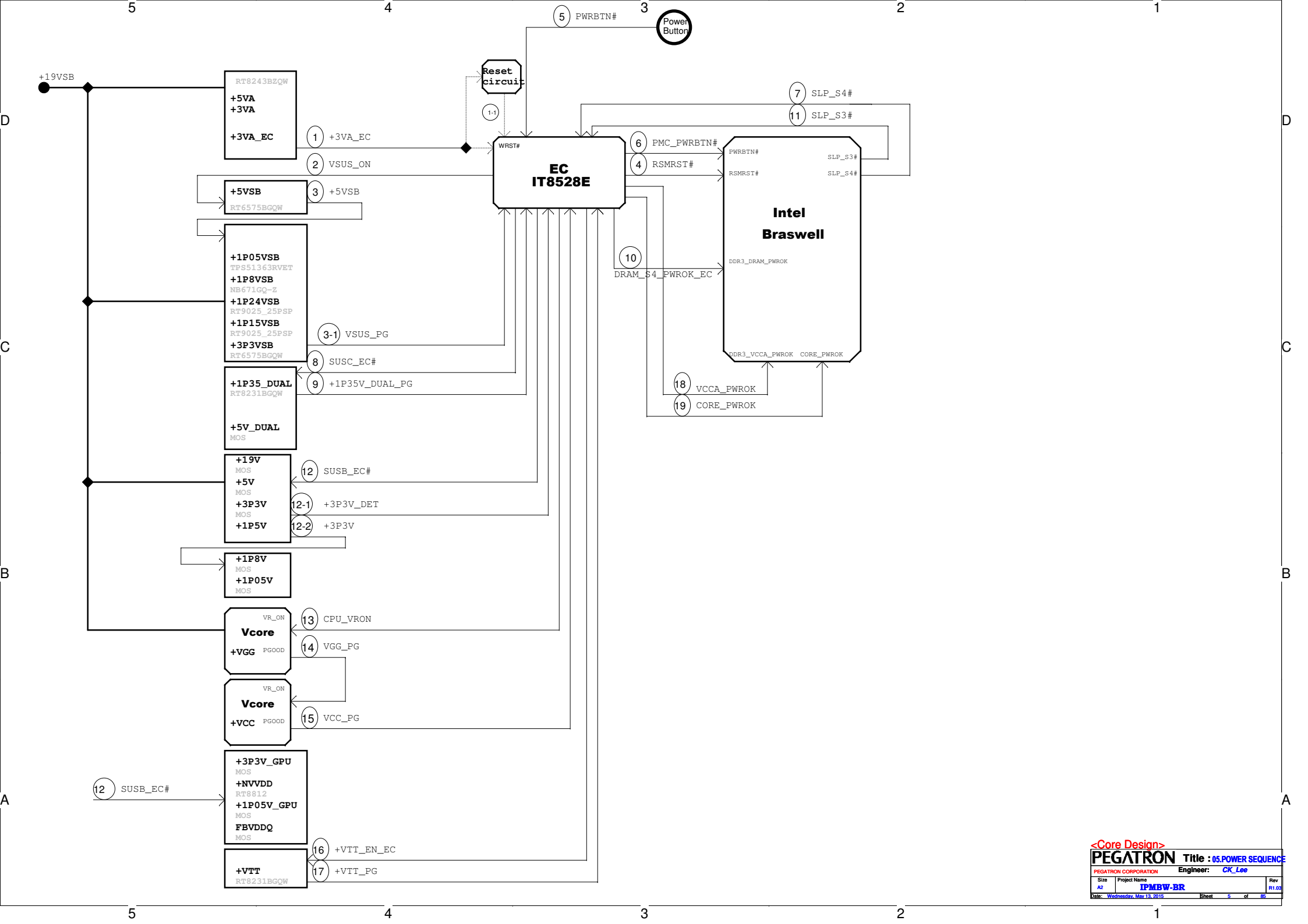


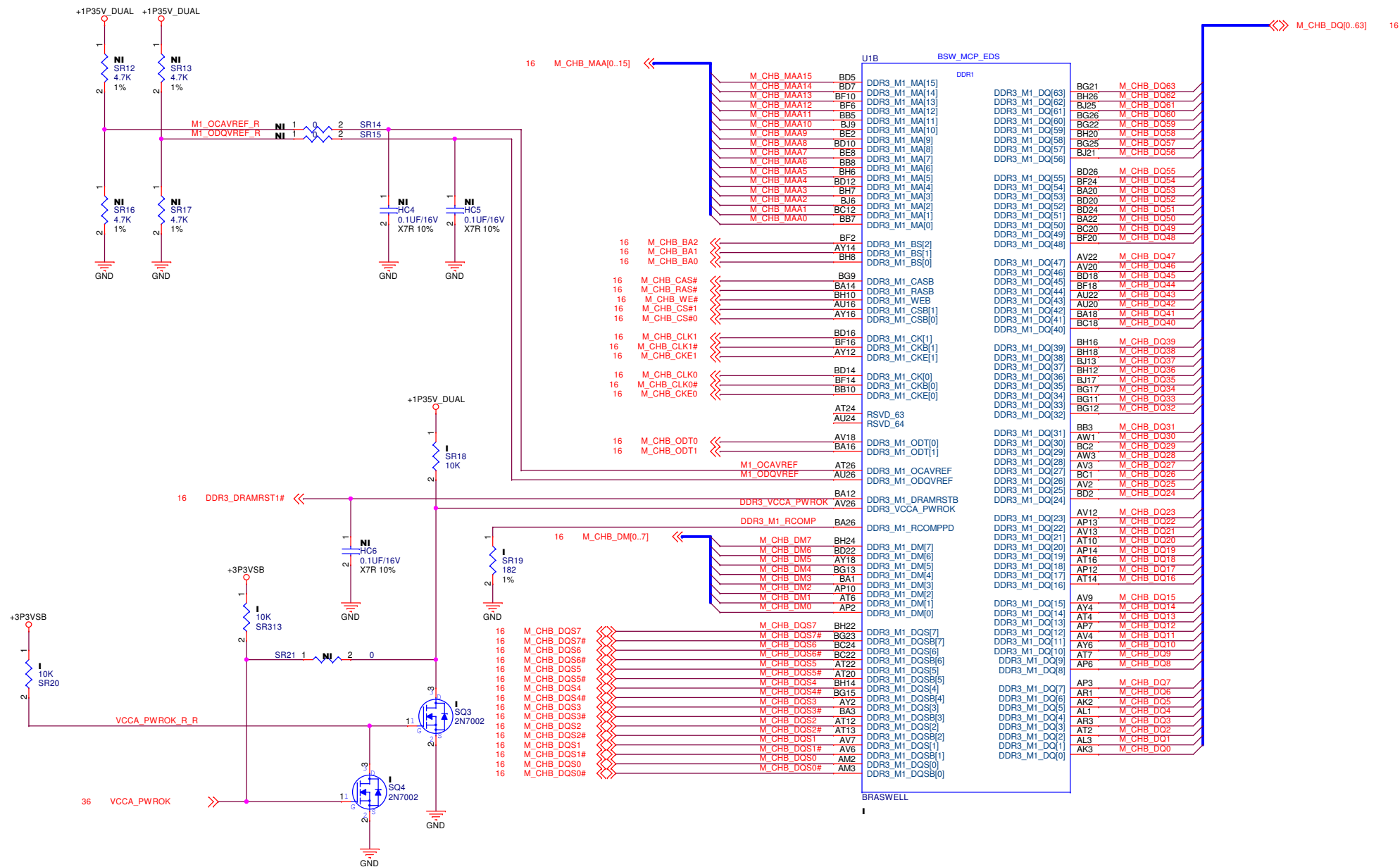
[illegible]

Schematics Change History

Version	Date	Comments







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PEGATRON Title : 07.SOC-2 DIMMB

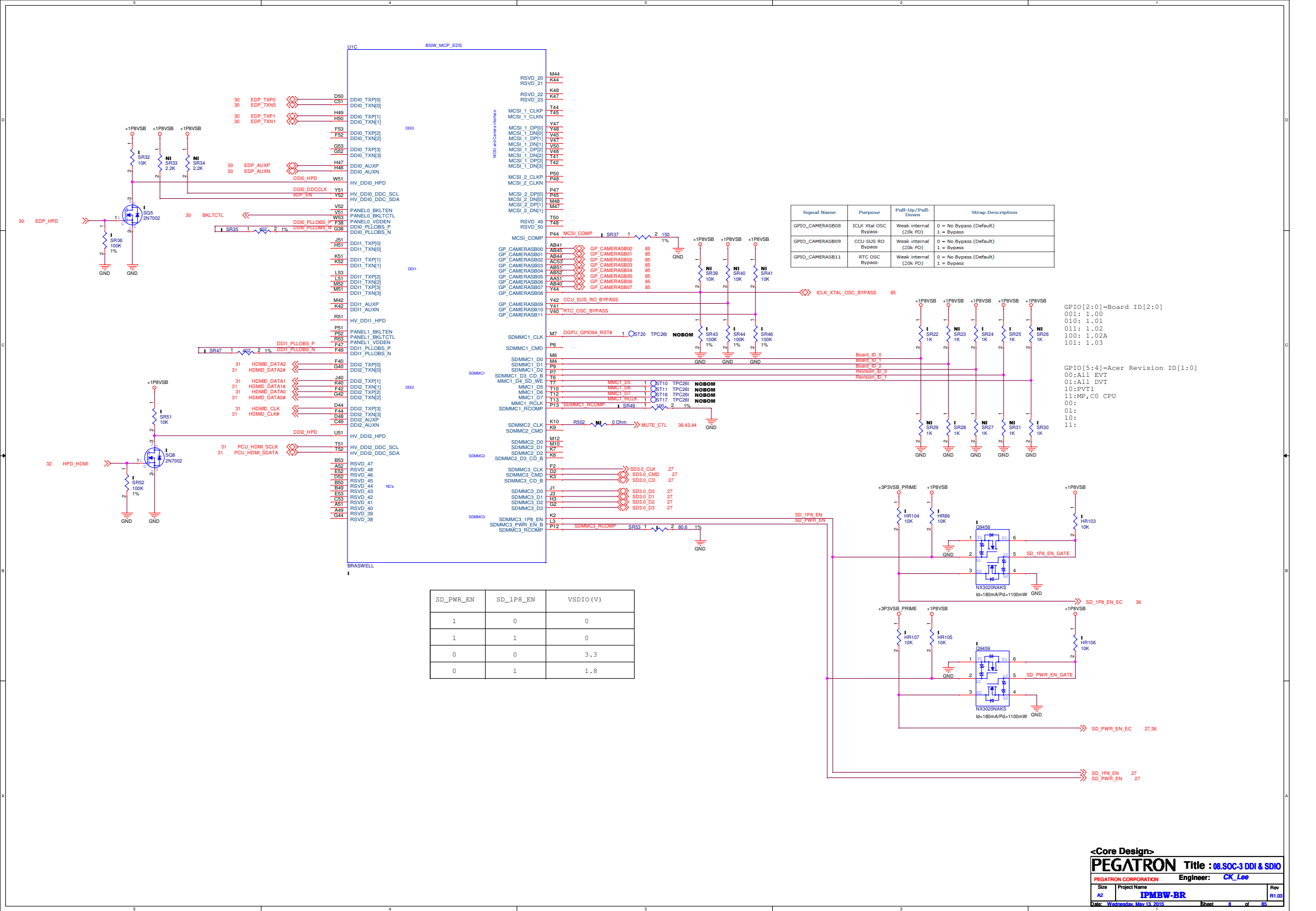
PEGATRON CORPORATION

Engineer: CK_Lee

Size A3	Project Name IPMBW-BR	Rev R1.03
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Date: Wednesday, May 13, 2015

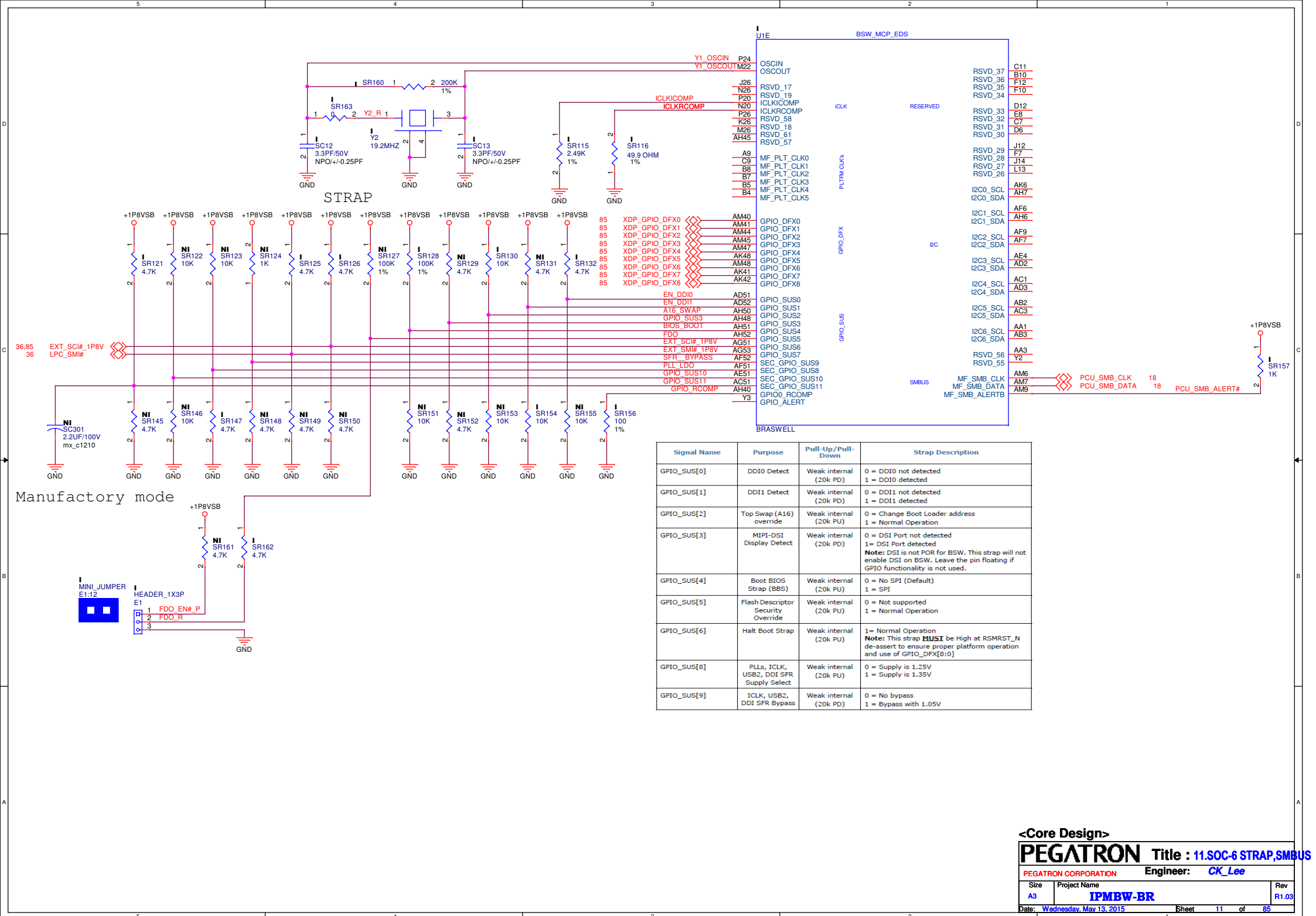
Sheet 7 of 85

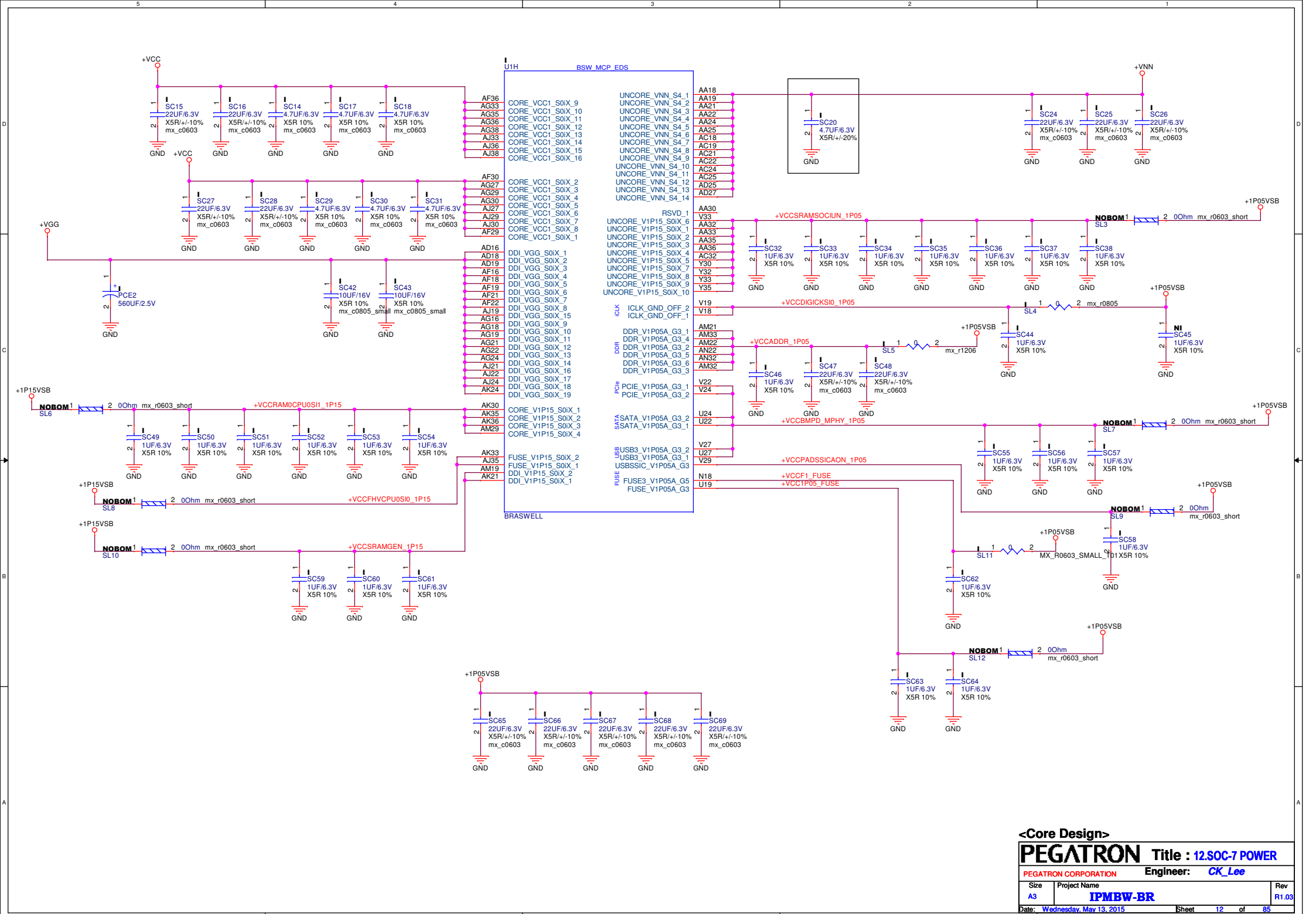


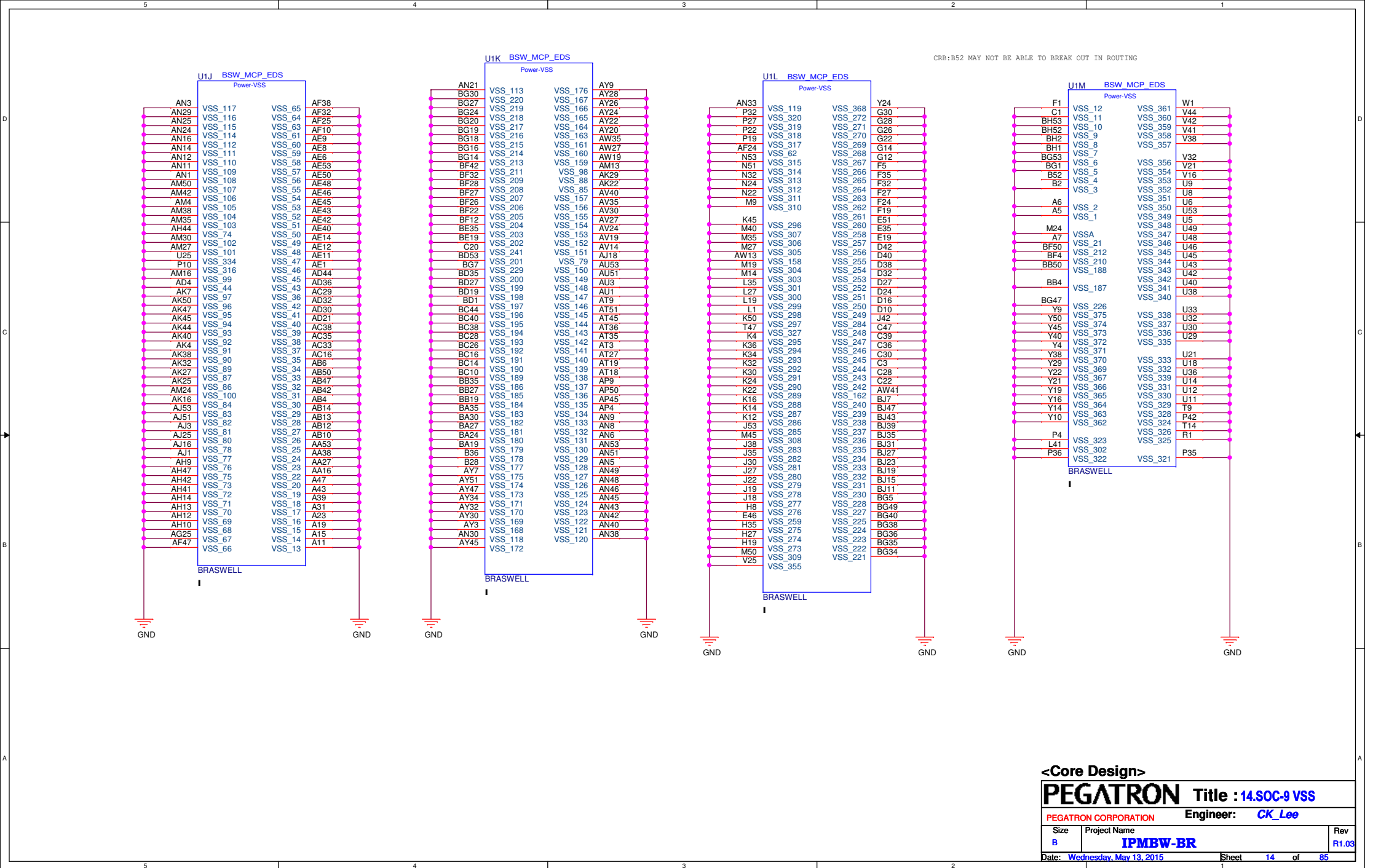
Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass

GPIO[2:0]=Board ID[2:0]
001: 1.00
010: 1.01
011: 1.02
100: 1.02A
101: 1.03

GPIO[5:4]=Acer Revision ID[1:0]
00:All EVT
01:All DVT
10:PVT1
11:MP,C0 CPU
00:
01:
10:
11:







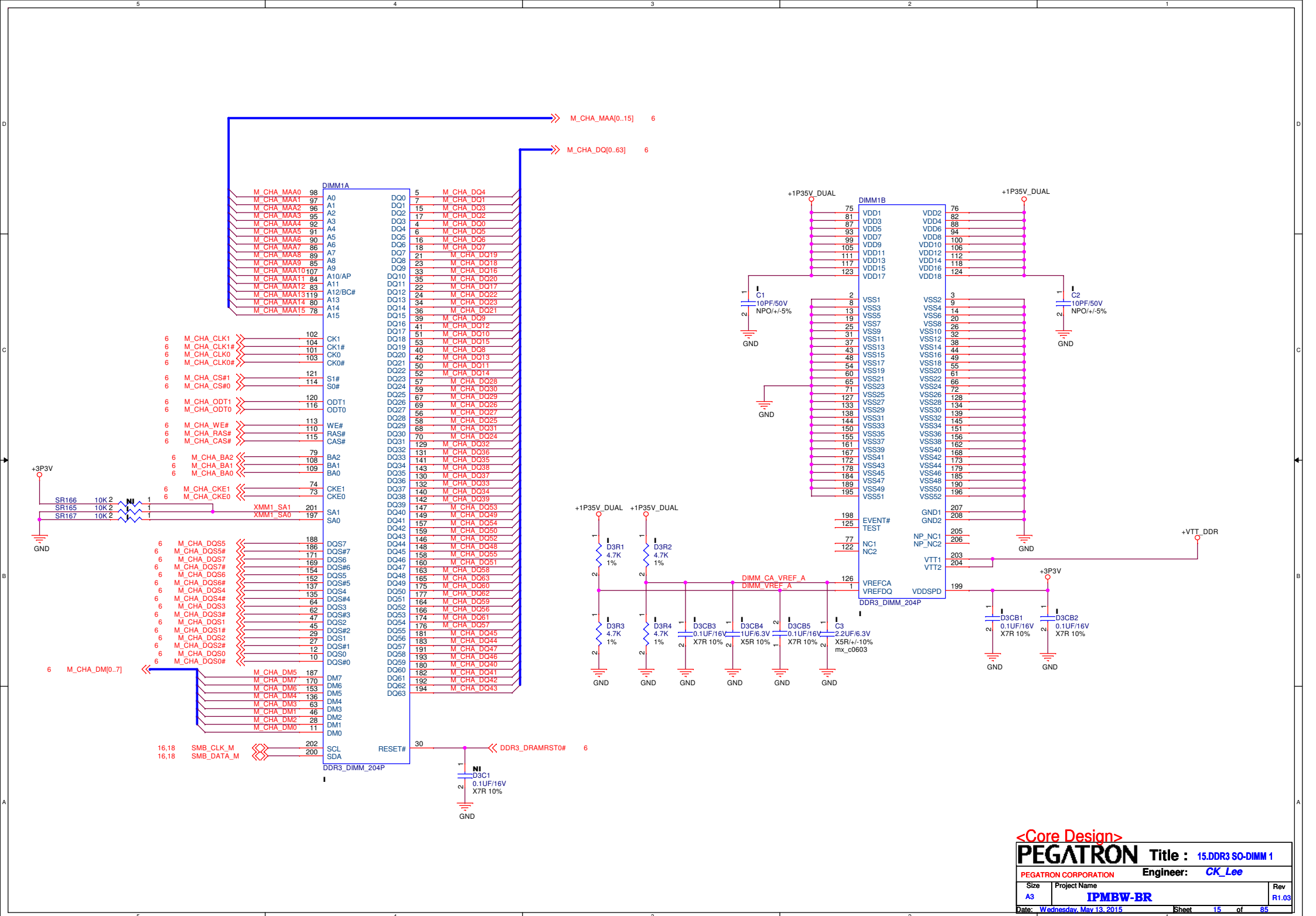
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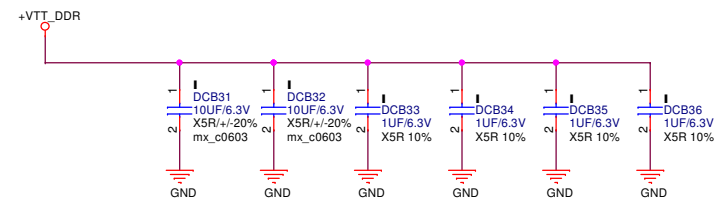
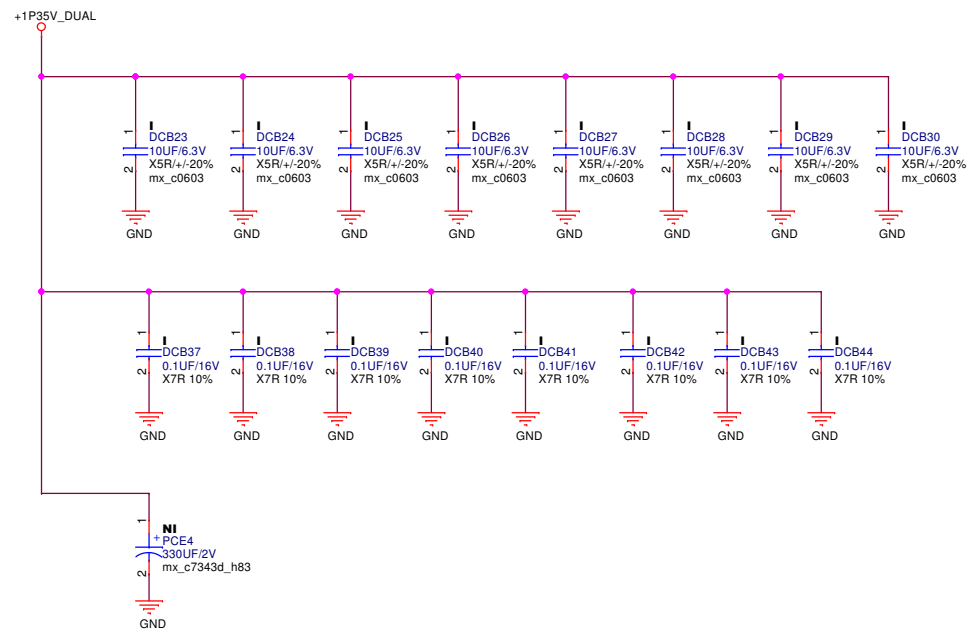
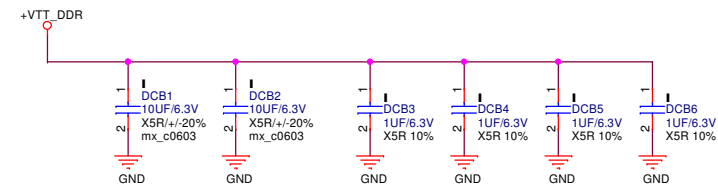
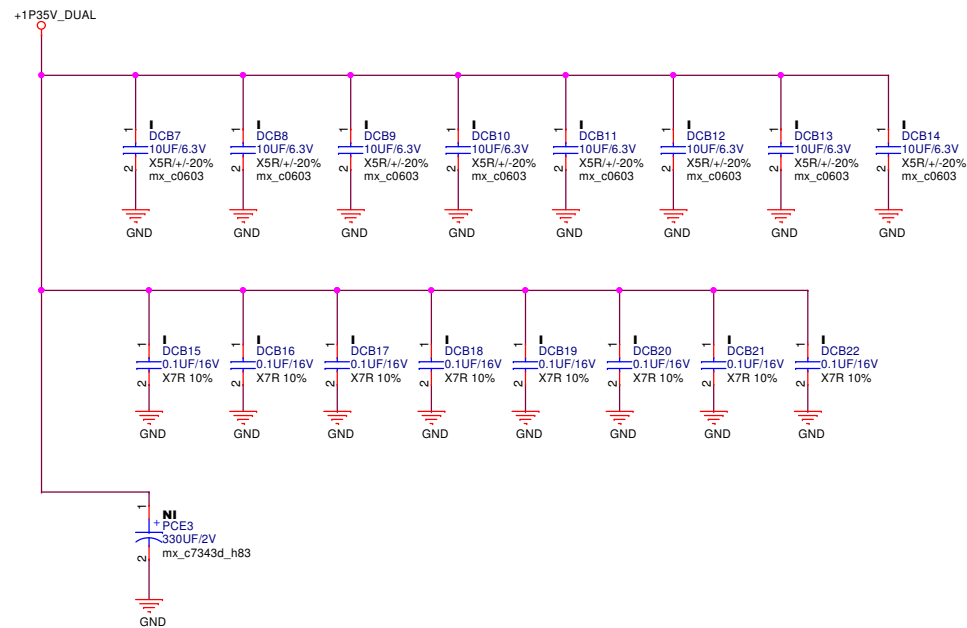
PEGATRON Title : 14.SOC-9 VSS

PEGATRON CORPORATION Engineer: CK_Lee

Size B	Project Name IPMBW-BR	Rev R1.03
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Date: Wednesday, May 13, 2015 Sheet 14 of 85





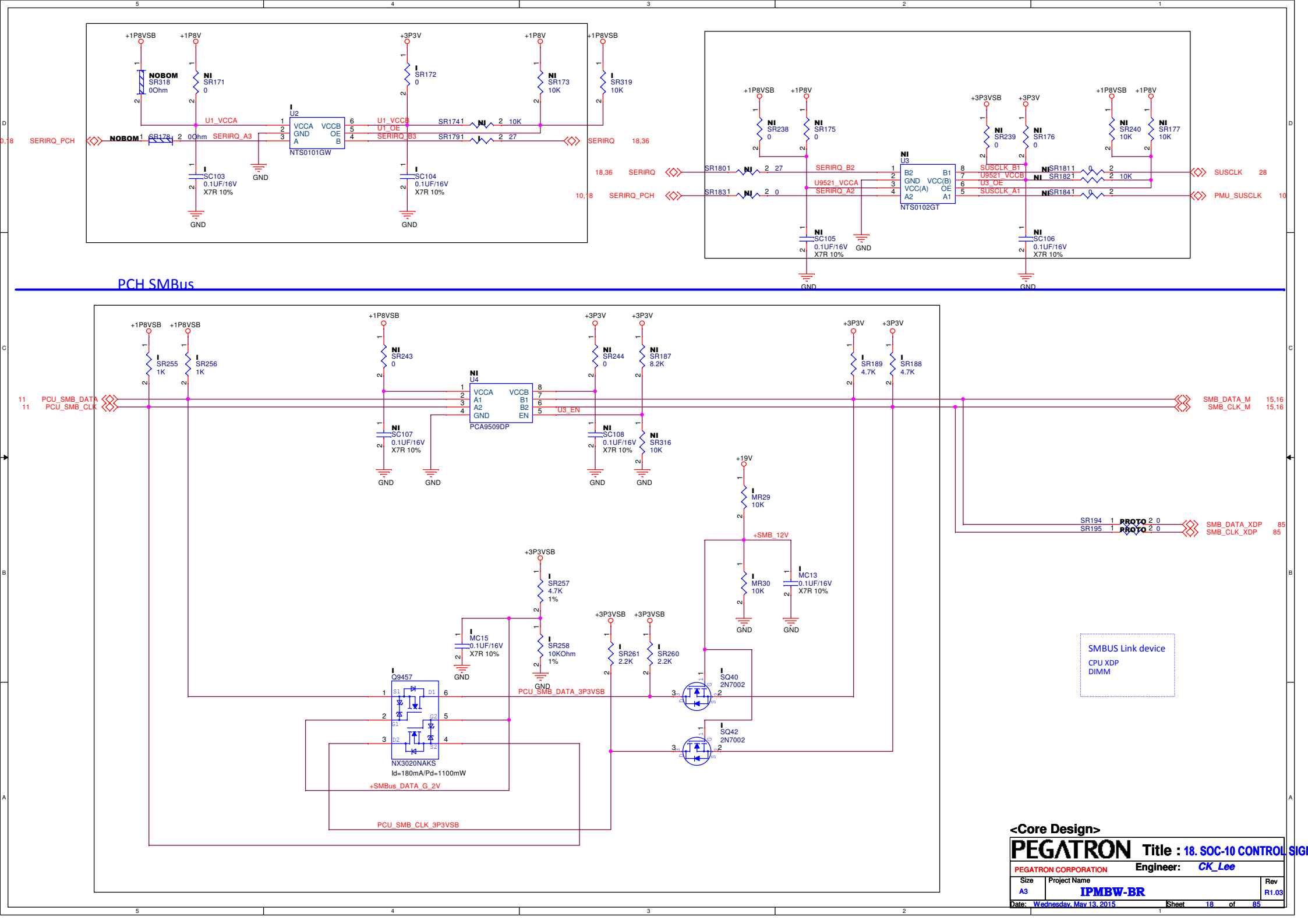
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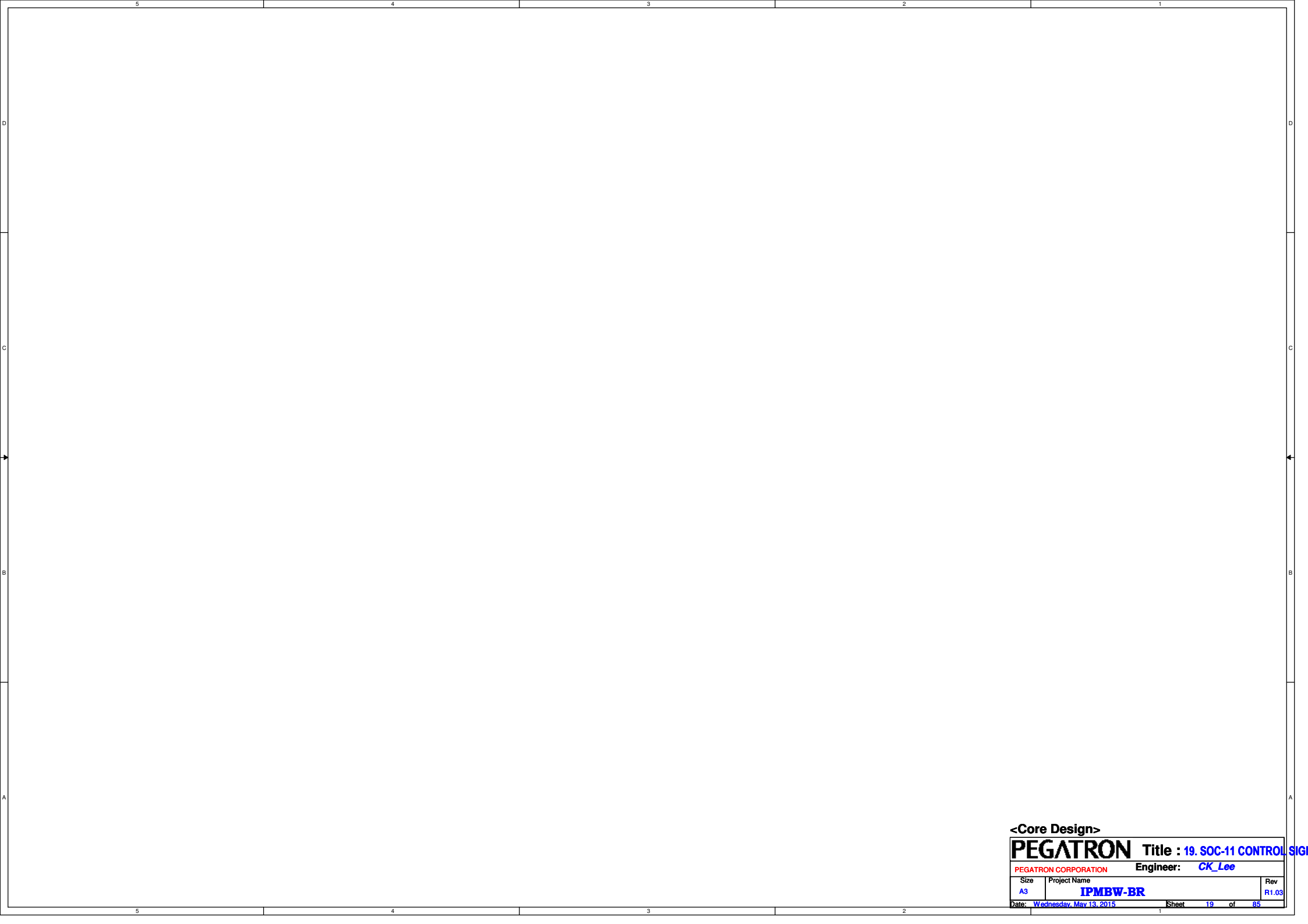
PEGATRON Title : 17.DDR3 TERMINATION A&B

PEGATRON CORPORATION Engineer: CK_Lee

Size A3	Project Name IPMBW-BR	Rev R1.03
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Date: Wednesday, May 13, 2015 Sheet 17 of 85

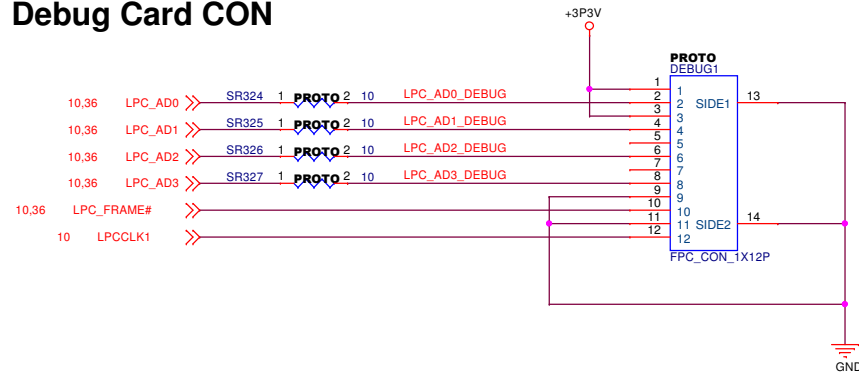




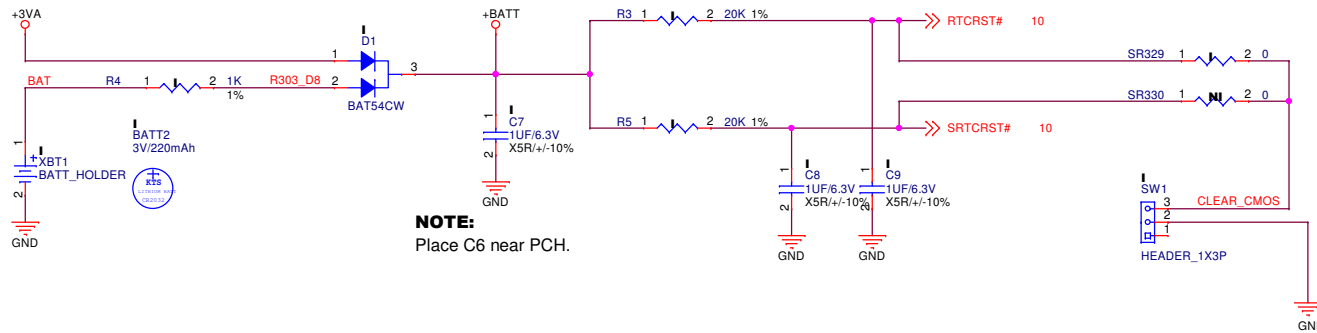
<Core Design>

PEGATRON		Title : 19. SOC-11 CONTROL SIGNAL	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size	Project Name	Rev	
A3	IPMBW-BR	R1.03	
Date: Wednesday, May 13, 2015		Sheet 19 of 85	

Debug Card CON

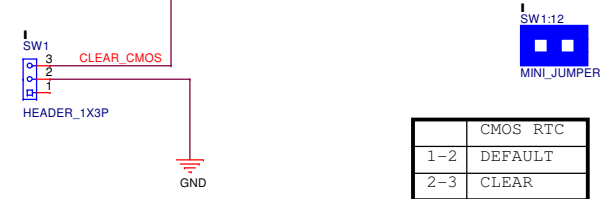


External RTC Circuitry



NOTE:
Place C6 near PCH.

CLR CMOS CIRCUIT



	CMOS RTC
1-2	DEFAULT
2-3	CLEAR

PEGATRON DT-MB RESTRICTED SECRET

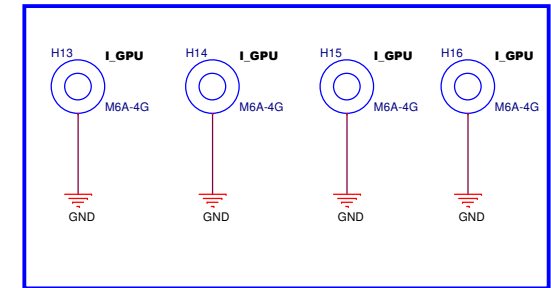
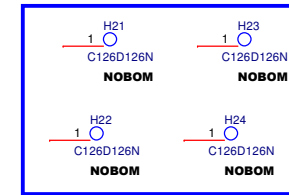
<Core Design>

PEGATRON		Title : 20.RTC/LPC DEBUG/CLR CMOS&PS	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size A3	Project Name IPMBW-BR		Rev R1.03
Date: Wednesday, May 13, 2015		Sheet 20 of 85	

PWM FAN

NUTS for Thermal (CPU)

NUTS for Thermal (GPU)



improve +VCC layout

place near CPU

place under dimm

place near Fan-IN

place near CPU

place under dimm

To EC RESET

<Core Design>

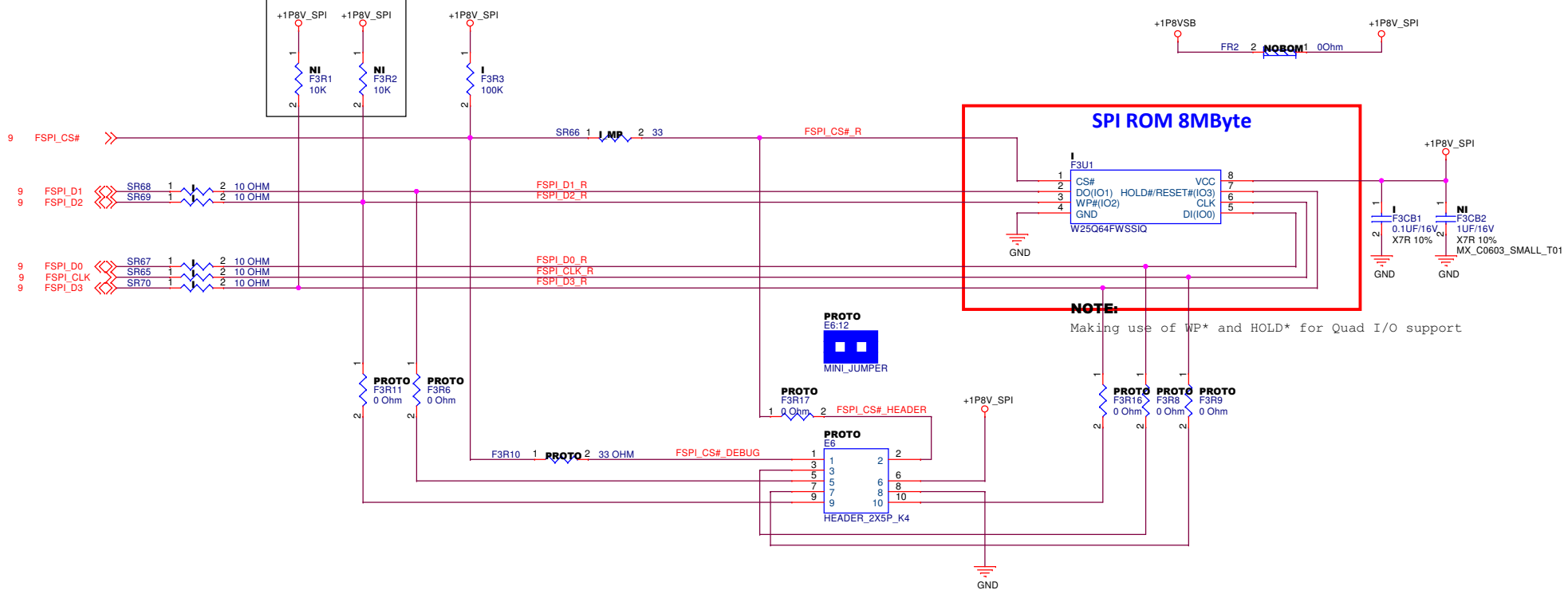
PEGATRON Title : 21.FAN/HEATSINKTherm

PEGATRON CORPORATION Engineer: CK_Lee

Size A3 Project Name IPMBW-BR Rev R1.03

Date: Wednesday, May 13, 2015 Sheet 21 of 85

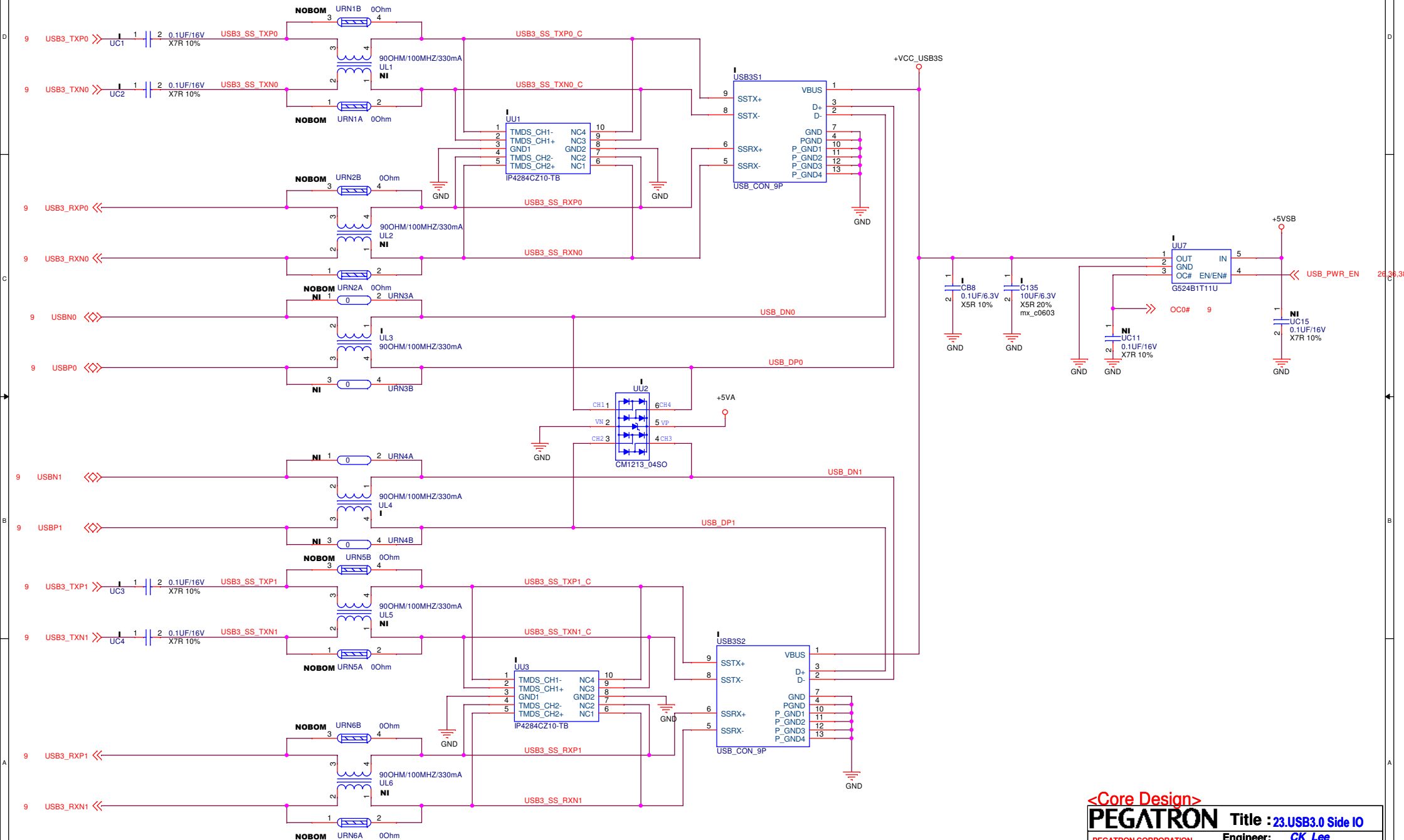
non-Quad IO will be I

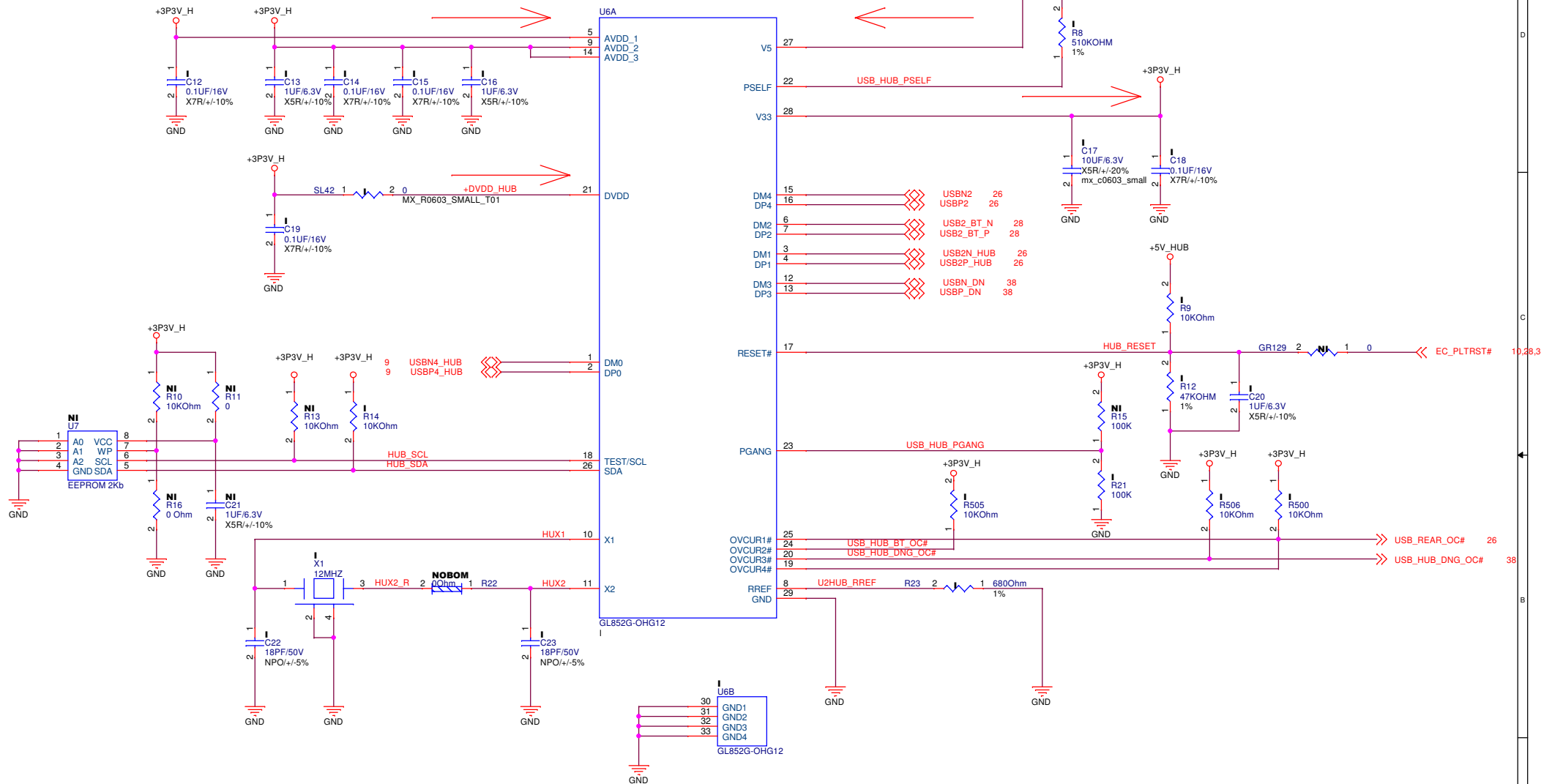


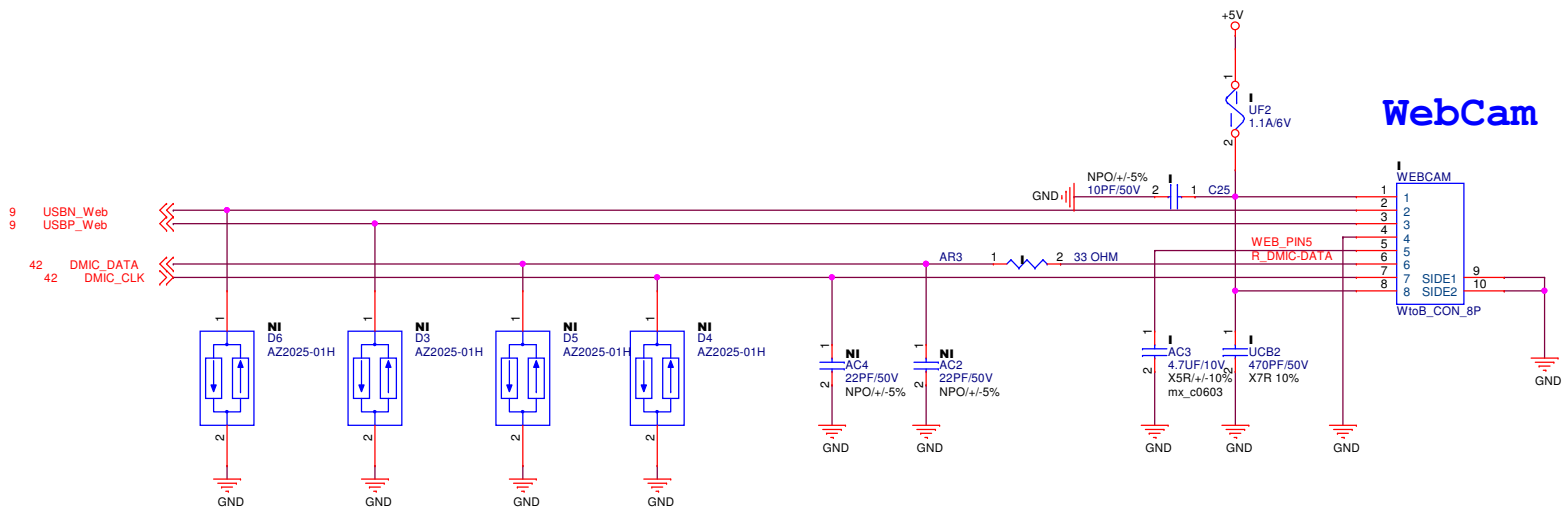
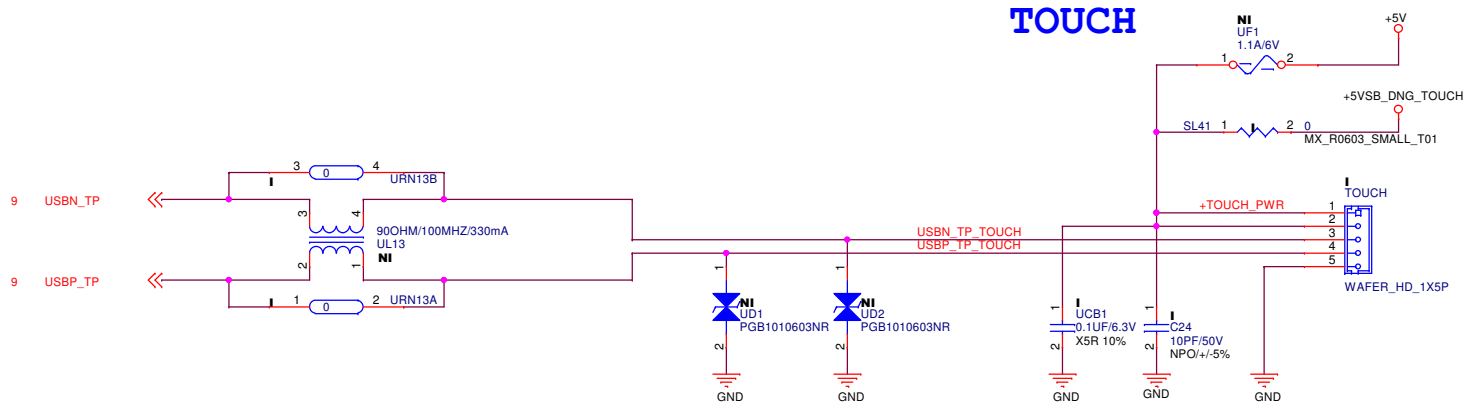
<Core Design>

PEGATRON		Title : 22.SPI ROM	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size A3	Project Name IPMBW-BR		Rev R1.03
Date: Wednesday, May 13, 2015		Sheet 22 of 85	

Side IO USB3.0







<Core Design>

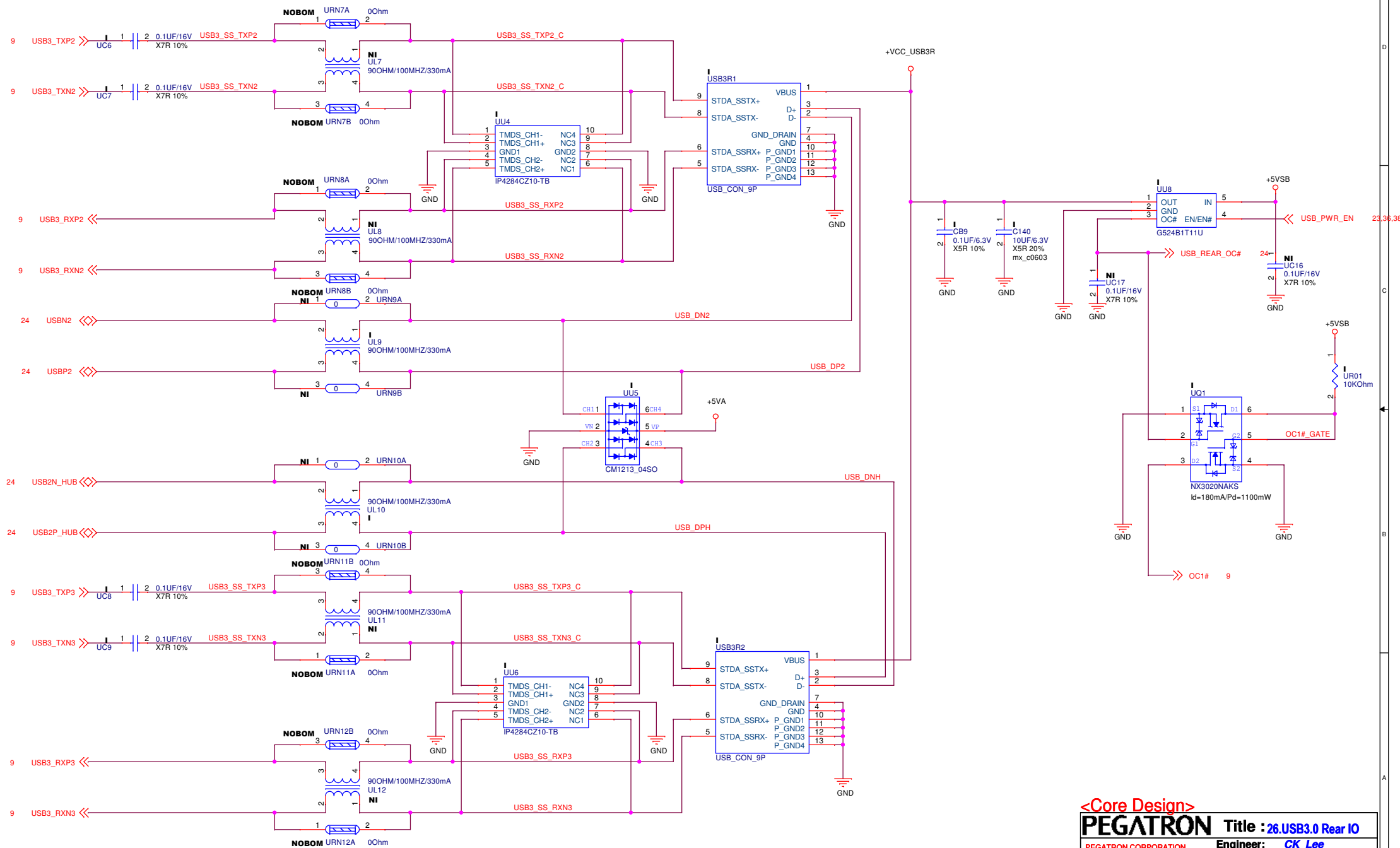
PEGATRON Title : 25.USB2.0 WebCam/Touch

PEGATRON CORPORATION Engineer: CK_Lee

Size A3 Project Name IPMBW-BR Rev R1.03

Date: Wednesday, May 13, 2015 Sheet 25 of 85

Rear IO USB3.0



<Core Design>

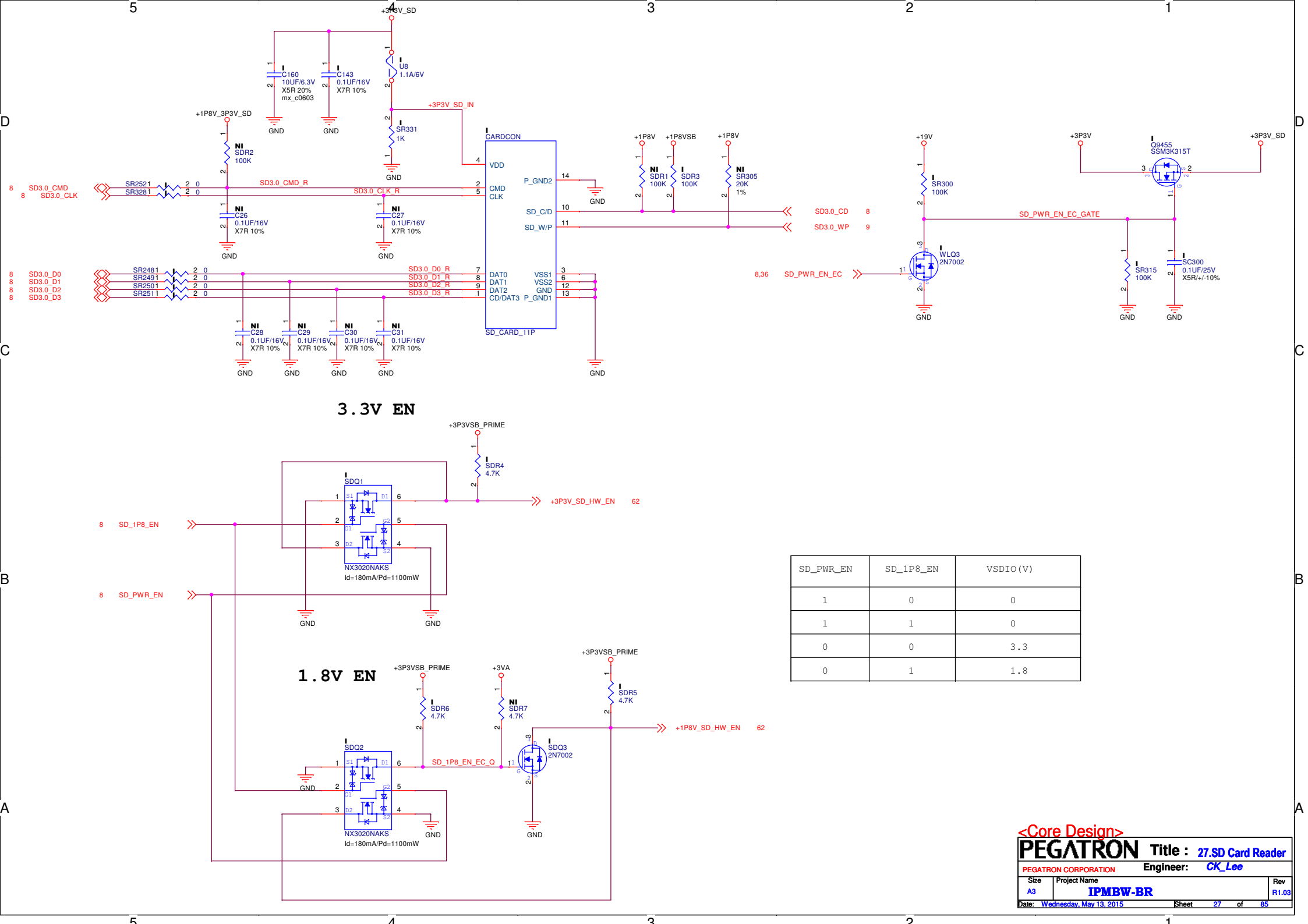
PEGATRON Title : 26.USB3.0 Rear IO

PEGATRON CORPORATION Engineer: CK_Lee

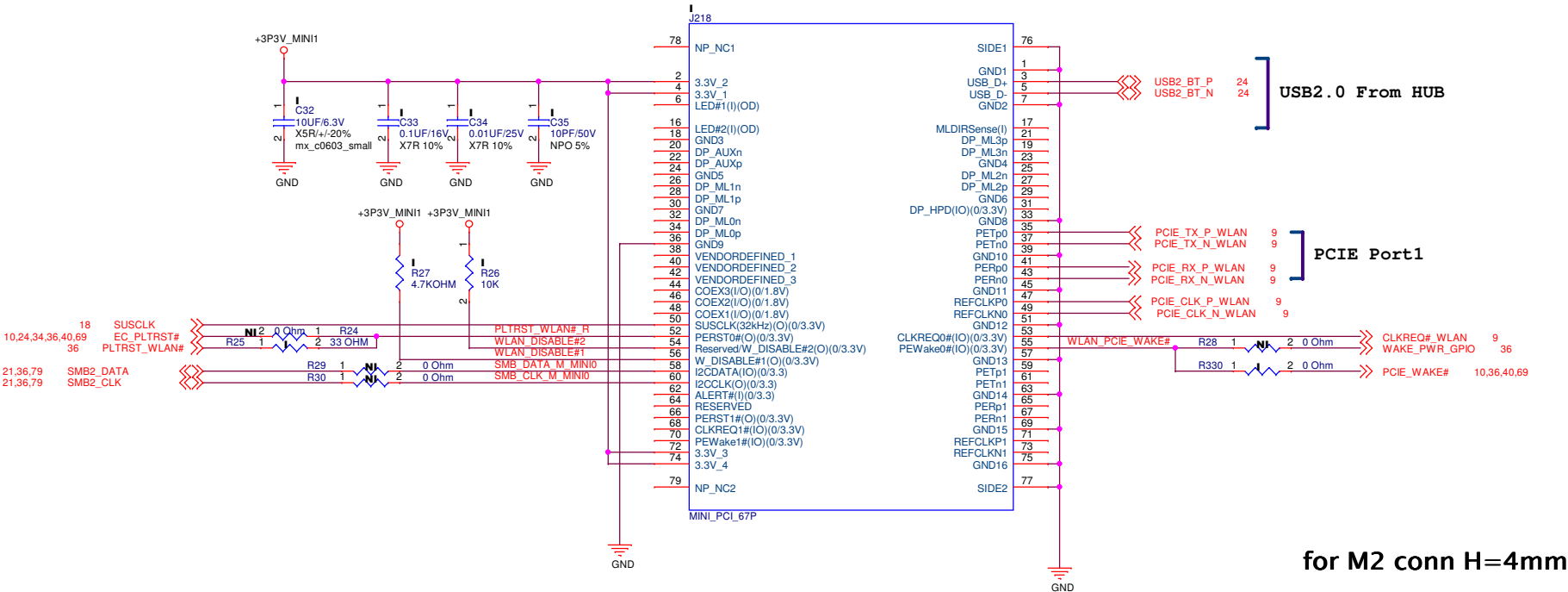
Size Project Name
A3 IPMBW-BR

Date: Wednesday, May 13, 2015 Sheet 26 of 85

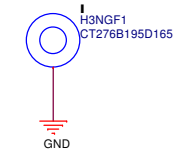
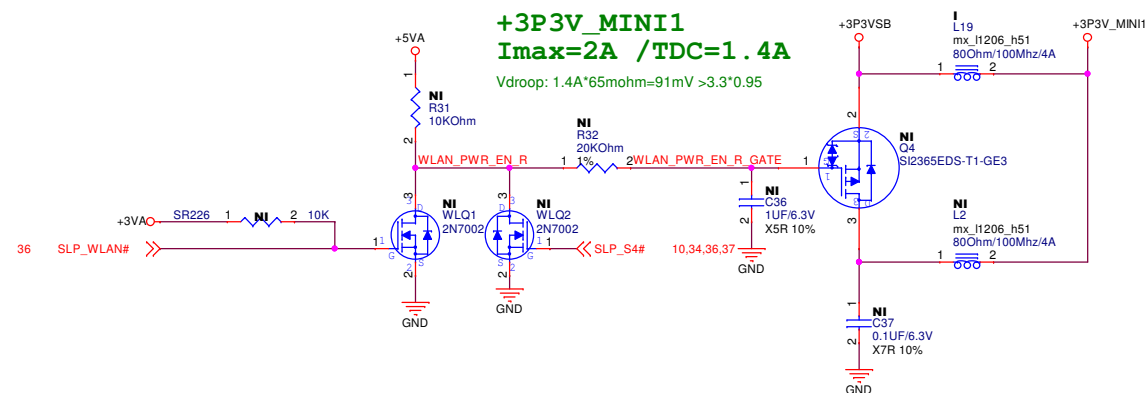
Rev
R1.03



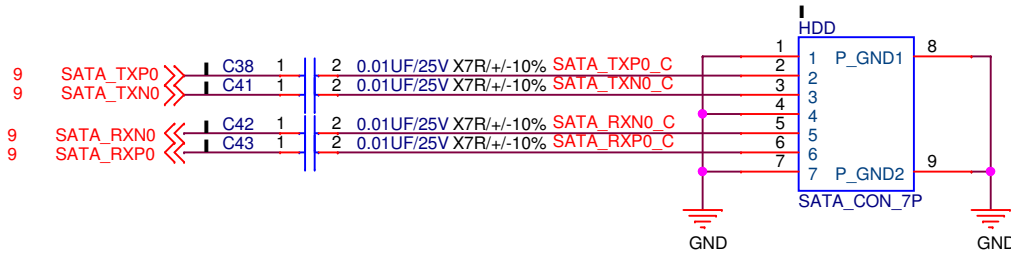
MiniCard for WiFi



for M2 conn H=4mm



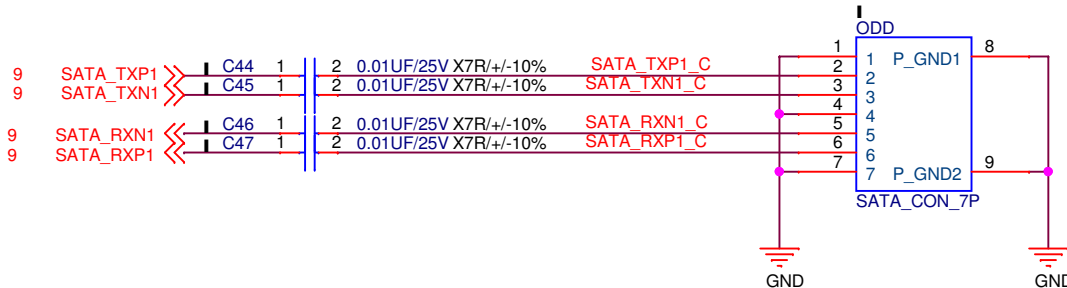
SATA HDD CON



**SATA CONTROLLER #1
(MASTER)**

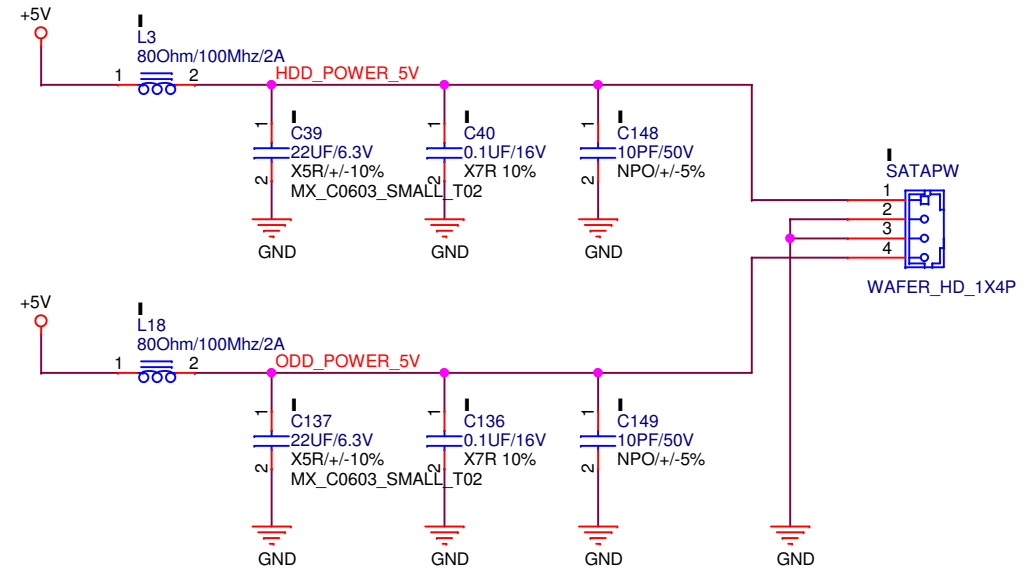
COLOR = DARK BLUE

SATA ODD CON



**SATA CONTROLLER #2
(SLAVE)**

SATA POWER CONN FOR HDD/ODD



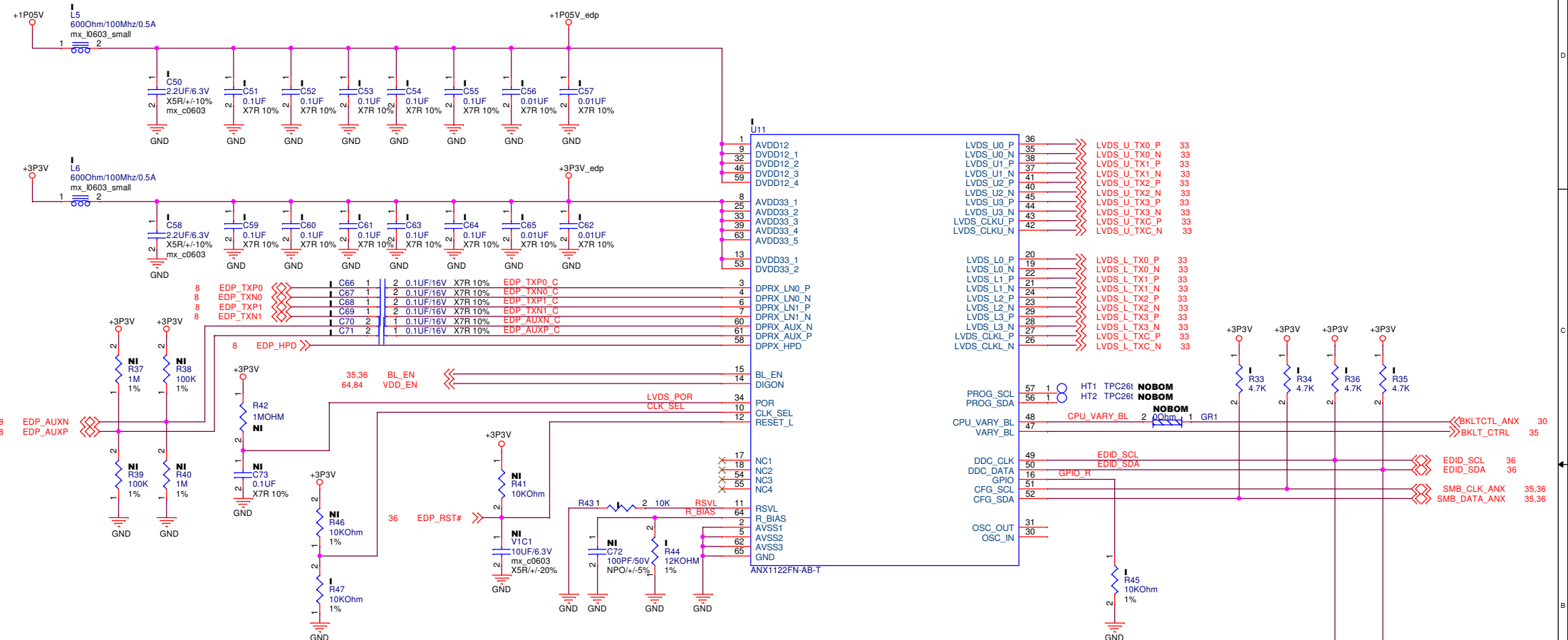
<Core Design>

PEGATRON Title : **29.SATA_HDD&ODD**

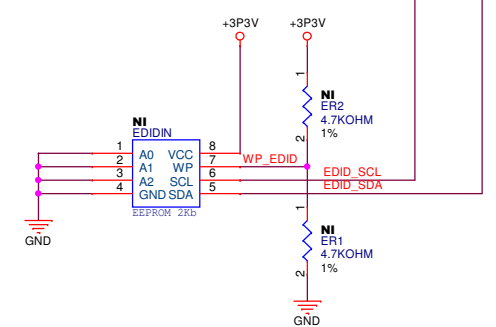
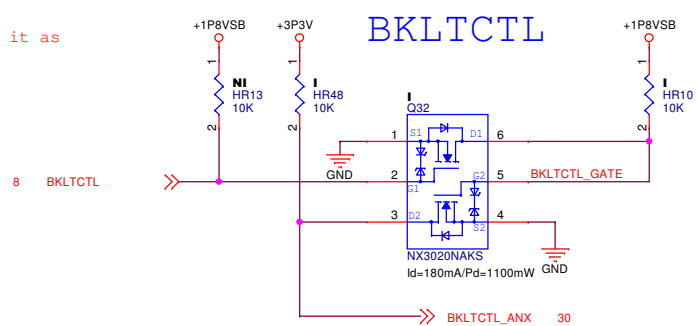
PEGATRON CORPORATION Engineer: **CK_Lee**

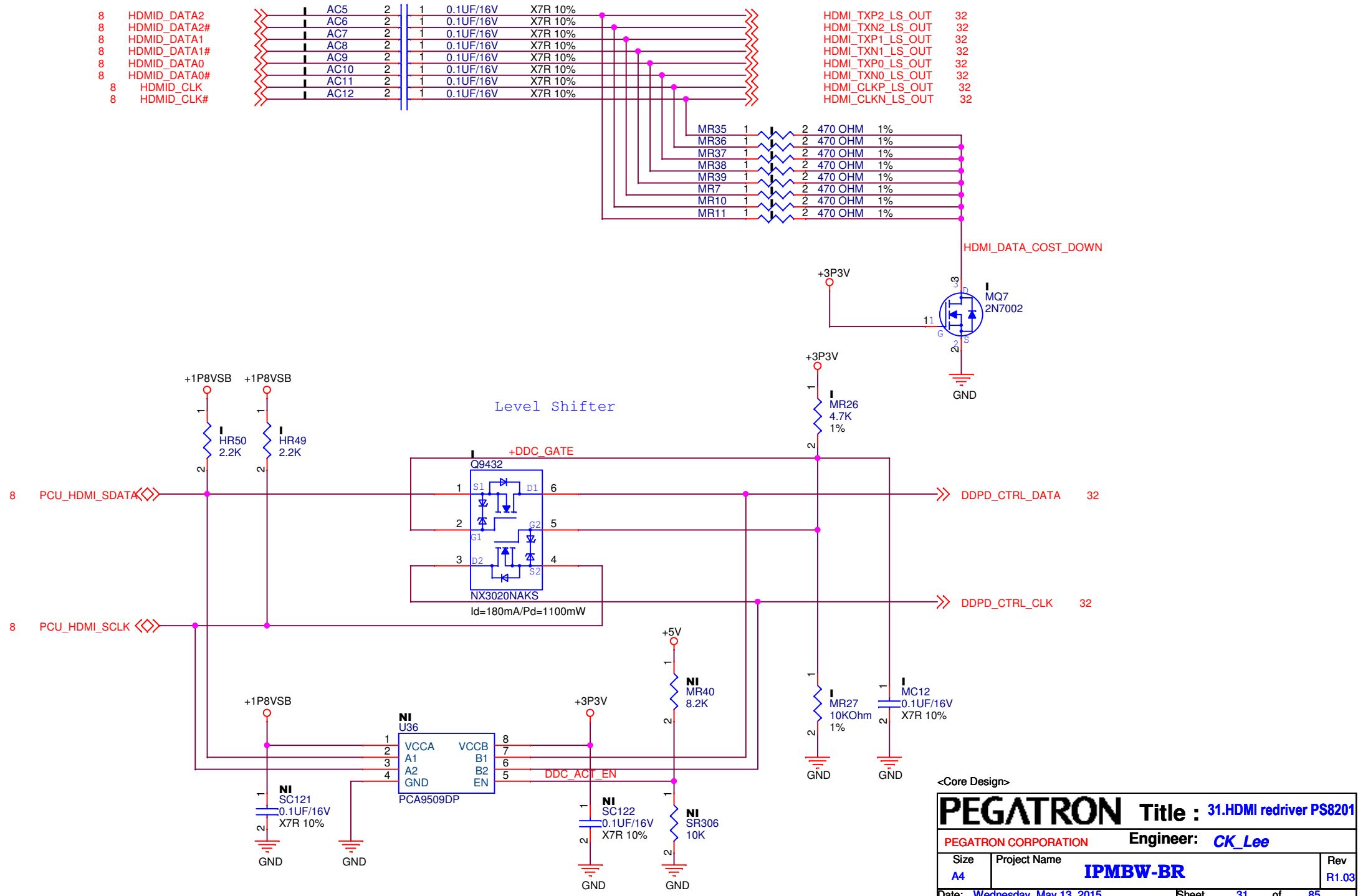
Size A4	Project Name IPMBW-BR	Rev R1.03
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Date: **Wednesday, May 13, 2015** Sheet **29** of **85**



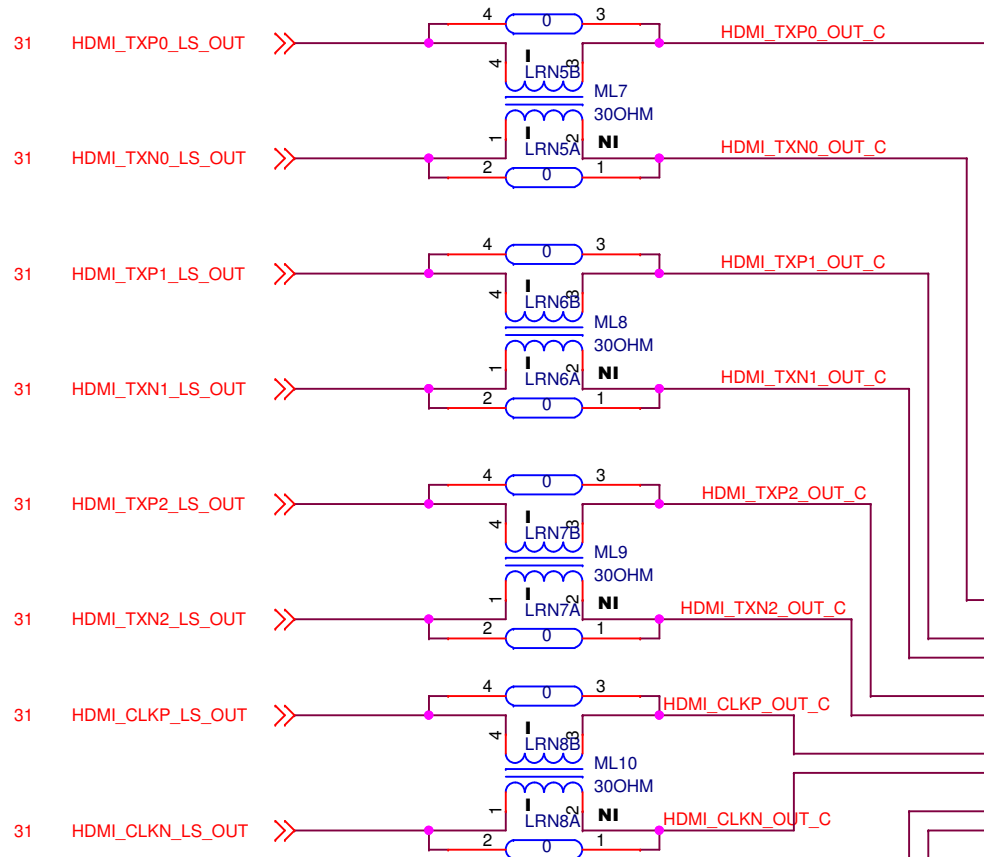
Input CLK selection
Pull up: work with 100M clock from Pin 30/31.
Pull down: work with on chip OSC and Pin 30/31 leave it as floating pin



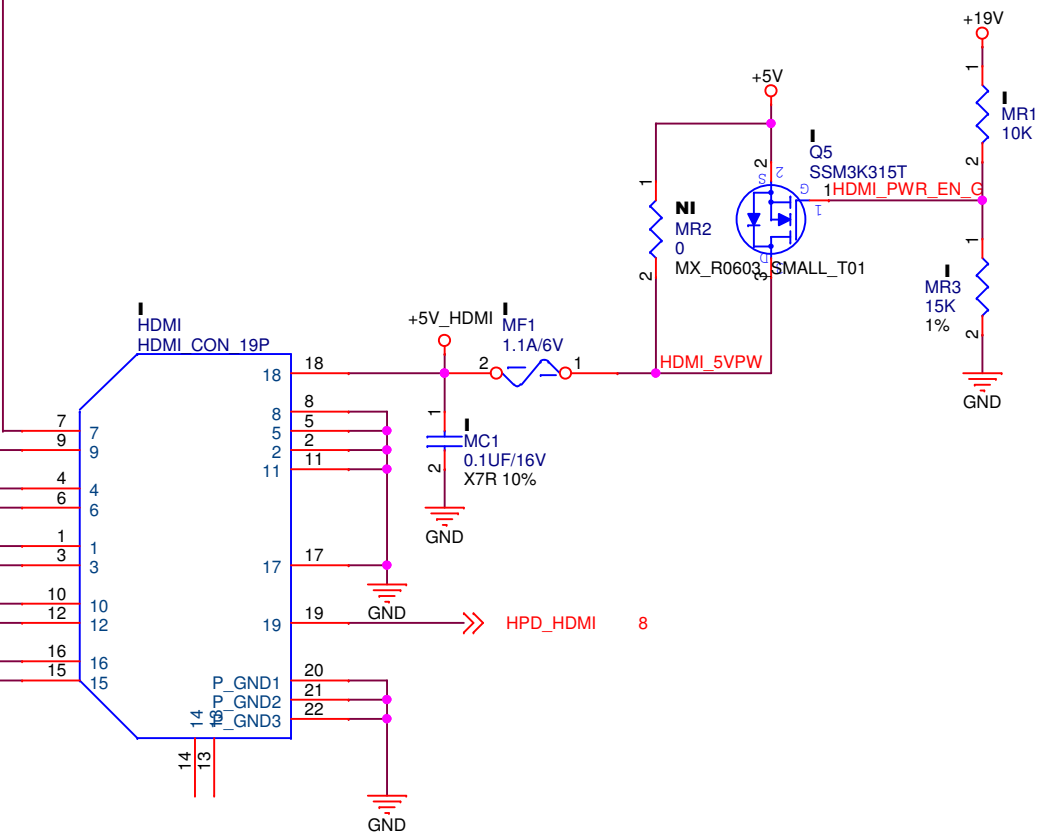
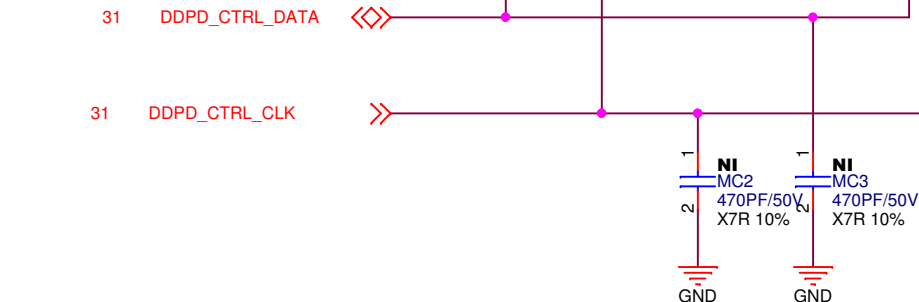
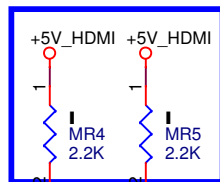


<Core Design>

PEGATRON		Title : 31.HDMI redriver PS8201	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size A4	Project Name IPMBW-BR		Rev R1.03
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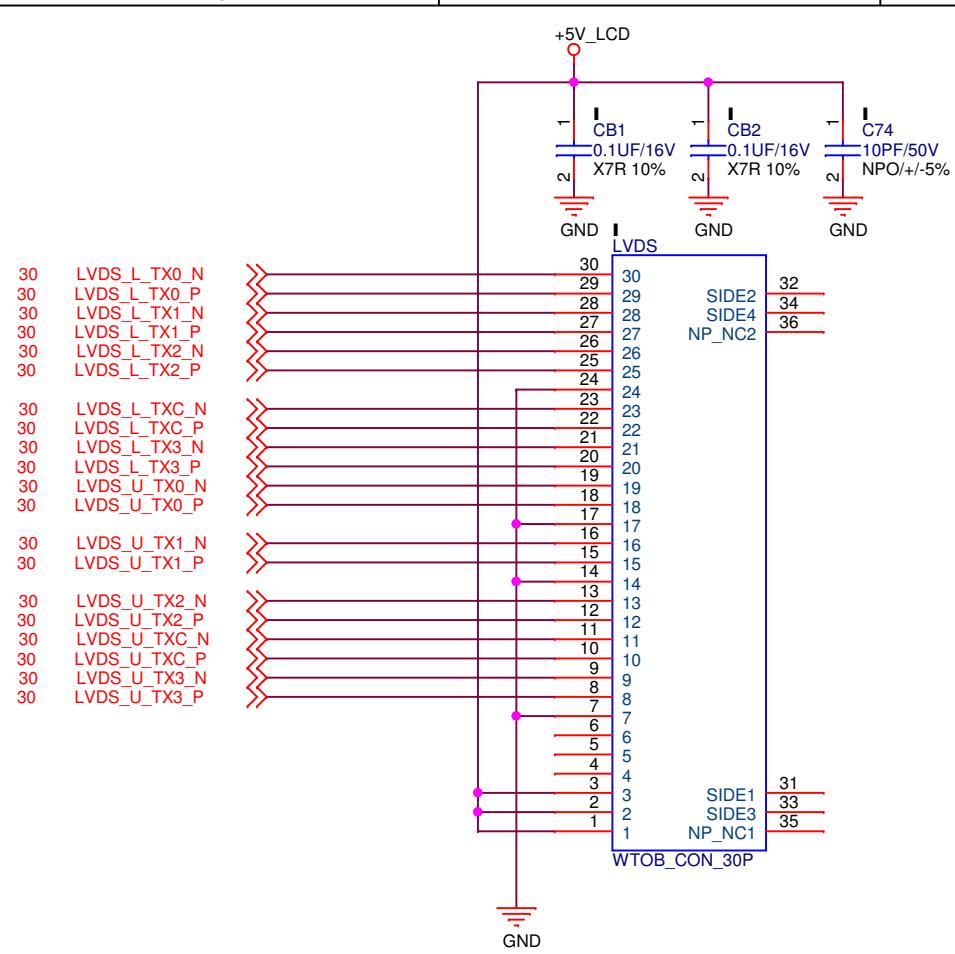


check APU side voltage level



<Core Design>

PEGATRON			Title : 32.HDMI OUT	
PEGATRON CORPORATION			Engineer: CK_Lee	
Size	Project Name			Rev
A4	IPMBW-BR			R1.03
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Pin	Name	Description
1	RXO0-	Negative LVDS differential data input. Channel O0 (odd)
2	RXO0+	Positive LVDS differential data input. Channel O0 (odd)
3	RXO1-	Negative LVDS differential data input. Channel O1 (odd)
4	RXO1+	Positive LVDS differential data input. Channel O1 (odd)
5	RXO2-	Negative LVDS differential data input. Channel O2 (odd)
6	RXO2+	Positive LVDS differential data input. Channel O2 (odd)
7	GND	Ground
8	RXOC-	Negative LVDS differential clock input. (odd)
9	RXOC+	Positive LVDS differential clock input. (odd)
10	RXO3-	Negative LVDS differential data input. Channel O3(odd)
11	RXO3+	Positive LVDS differential data input. Channel O3 (odd)
12	RXE0-	Negative LVDS differential data input. Channel E0 (even)
13	RXE0+	Positive LVDS differential data input. Channel E0 (even)
14	GND	Ground
15	RXE1-	Negative LVDS differential data input. Channel E1 (even)
16	RXE1+	Positive LVDS differential data input. Channel E1 (even)
17	GND	Ground
18	RXE2-	Negative LVDS differential data input. Channel E2 (even)
19	RXE2+	Positive LVDS differential data input. Channel E2 (even)
20	RXEC-	Negative LVDS differential clock input. (even)
21	RXEC+	Positive LVDS differential clock input. (even)
22	RXE3-	Negative LVDS differential data input. Channel E3 (even)
23	RXE3+	Positive LVDS differential data input. Channel E3 (even)

24	GND	Ground
25	NC	For LCD internal use only, Do not connect
26	NC	For LCD internal use only, Do not connect
27	NC	For LCD internal use only, Do not connect
28	Vcc	+5.0V power supply
29	Vcc	+5.0V power supply
30	Vcc	+5.0V power supply

<Core Design>

PEGATRON

Title : 33.LVDS CON/Panel Power

PEGATRON CORPORATION

Engineer: CK_Lee

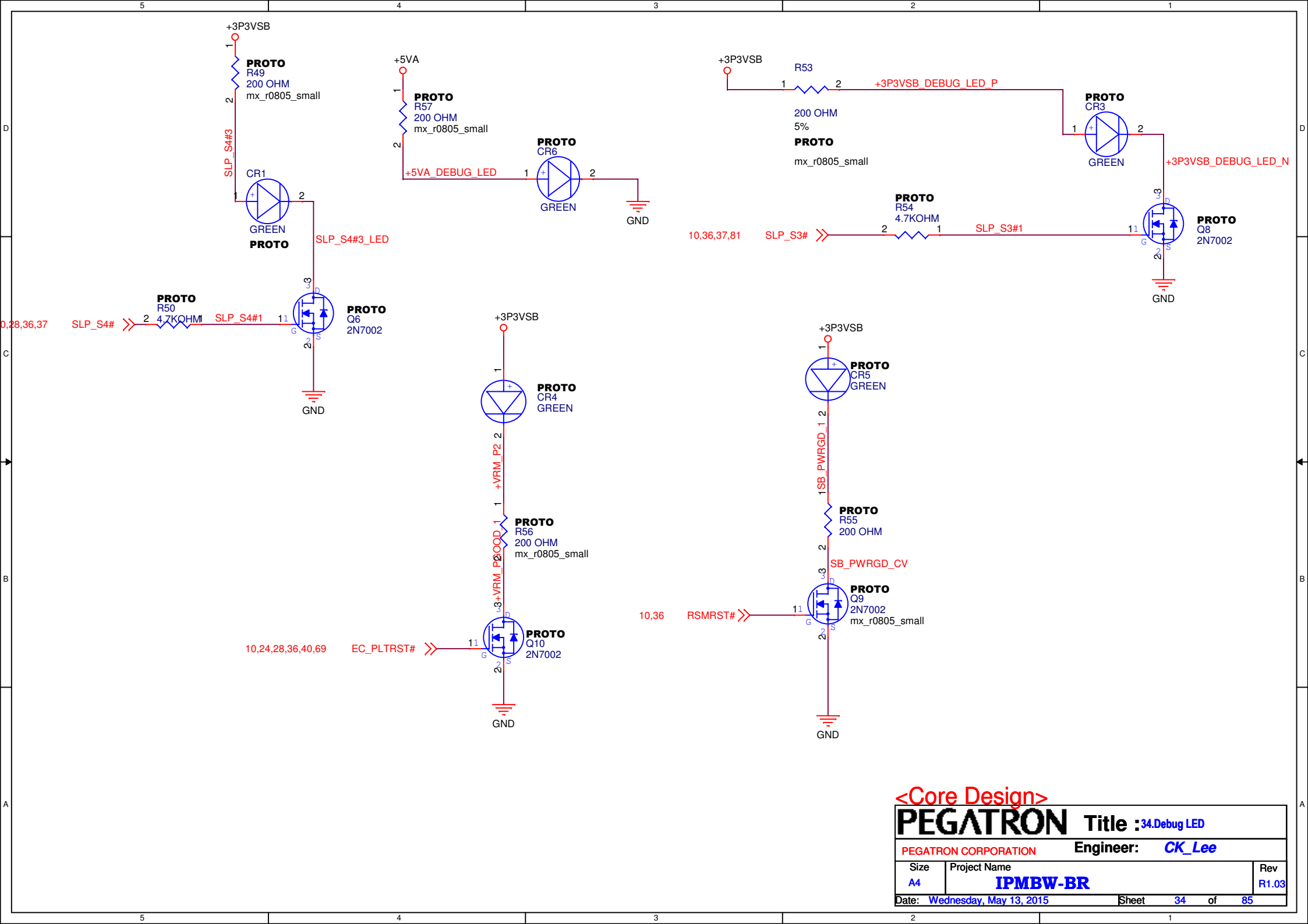
SizeA4

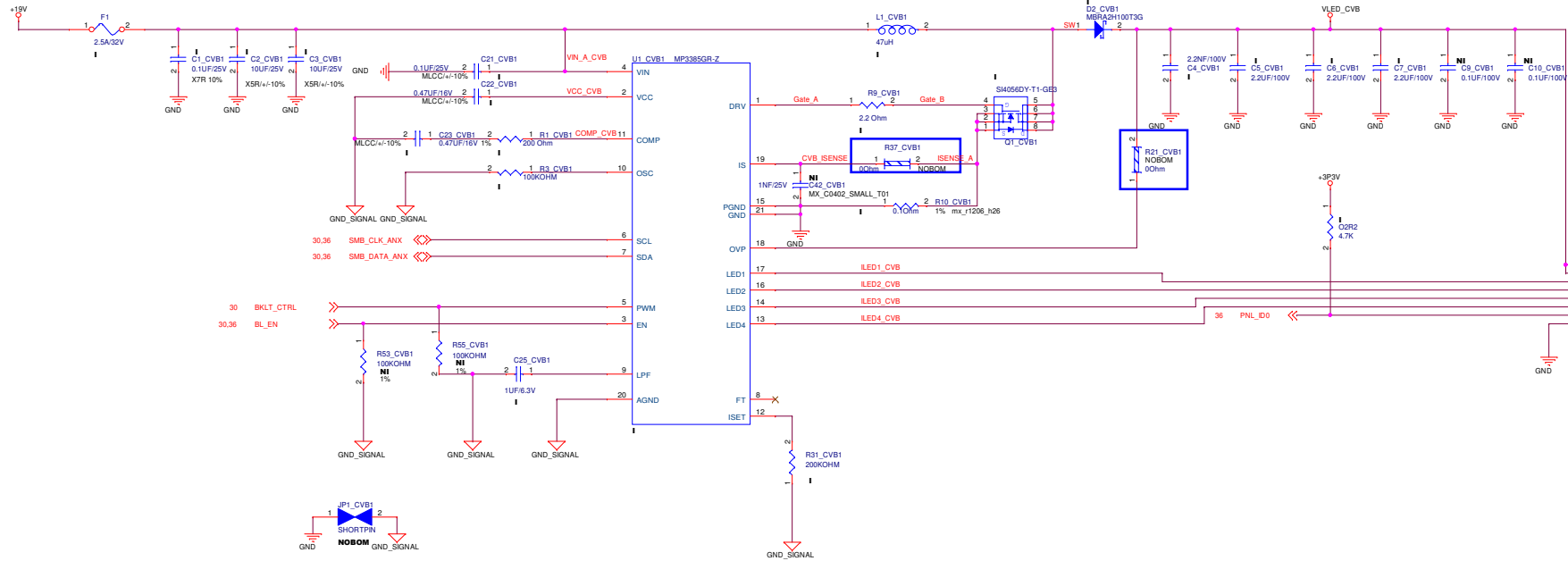
Project NameIPMBW-BR

RevR1.03

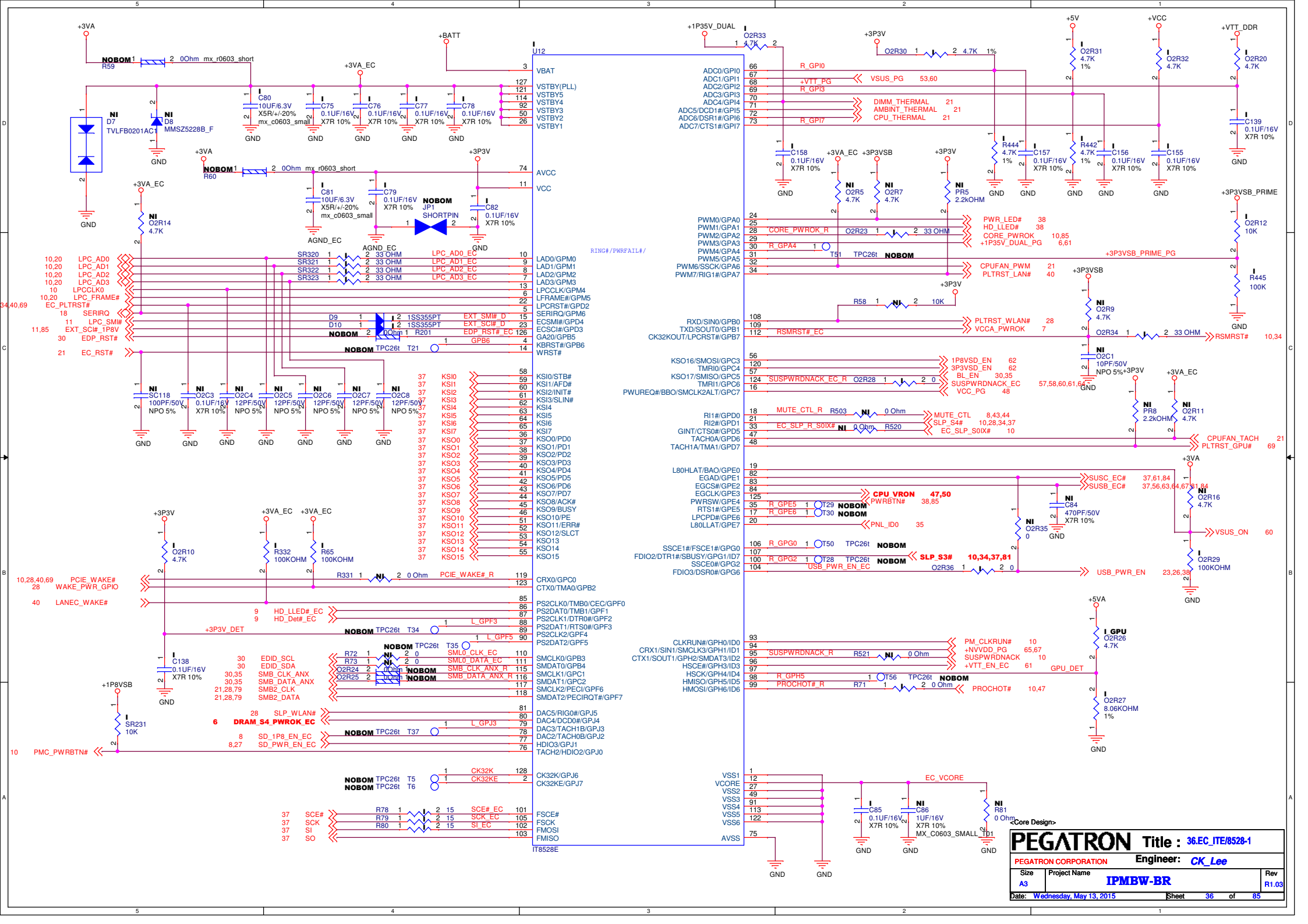
Date: Wednesday, May 13, 2015

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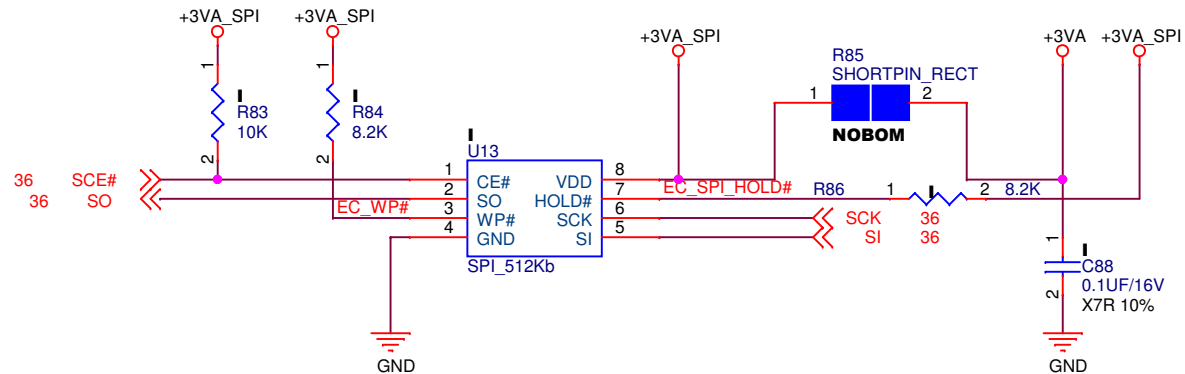




BL_EN	NOROM1	TPC26T
SMB_CLK_ANX	NOROM1	TPC26T
SMB_DATA_ANX	NOROM1	TPC26T
BKLT_CTRL	NOROM1	TPC26T
GND	NOROM1	TPC26T
VLED_CVB	NOROM1	TPC26T
ILED1_CVB	NOROM1	TPC26T
ILED2_CVB	NOROM1	TPC26T
ILED3_CVB	NOROM1	TPC26T
ILED4_CVB	NOROM1	TPC26T
PNL_ID0	NOROM1	TPC26T
GND	NOROM1	TPC26T
GND	NOROM1	TPC26T
GND	NOROM1	TPC26T
GND	NOROM1	TPC26T
GND	NOROM1	TPC26T



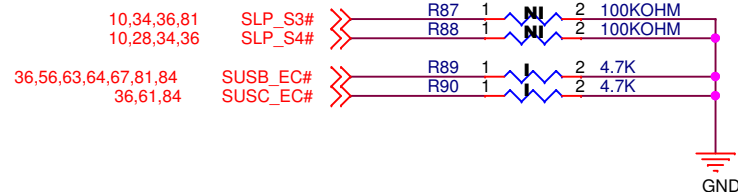
SPI ROM+ External programming conn.



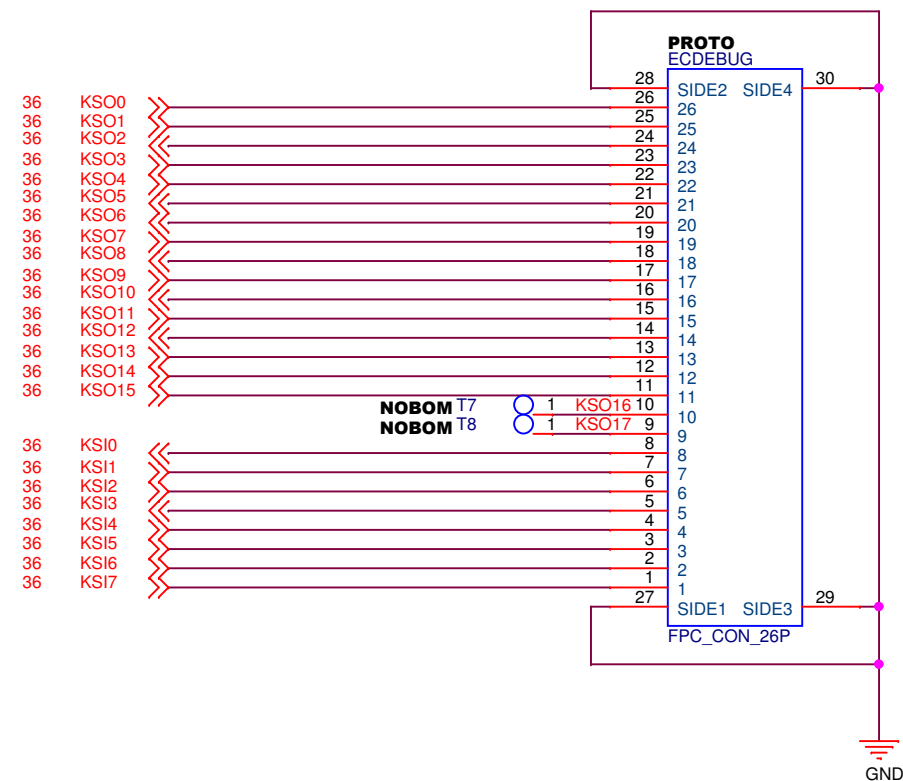
For EC PU/PD

05X00Z2FC330 32Mb

0500-00P5000 (512Kb SPI)



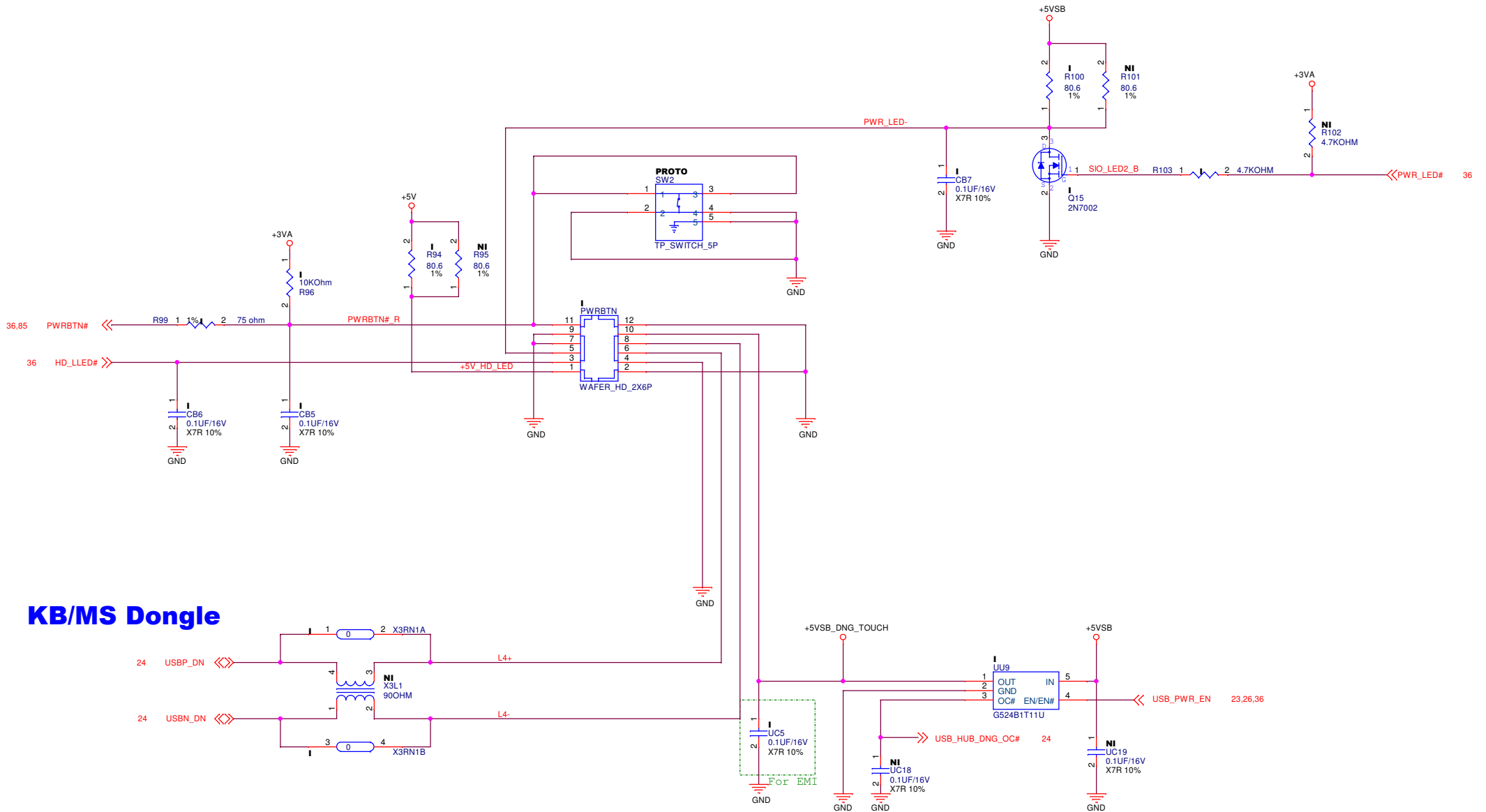
Keyboard Connector(debug)

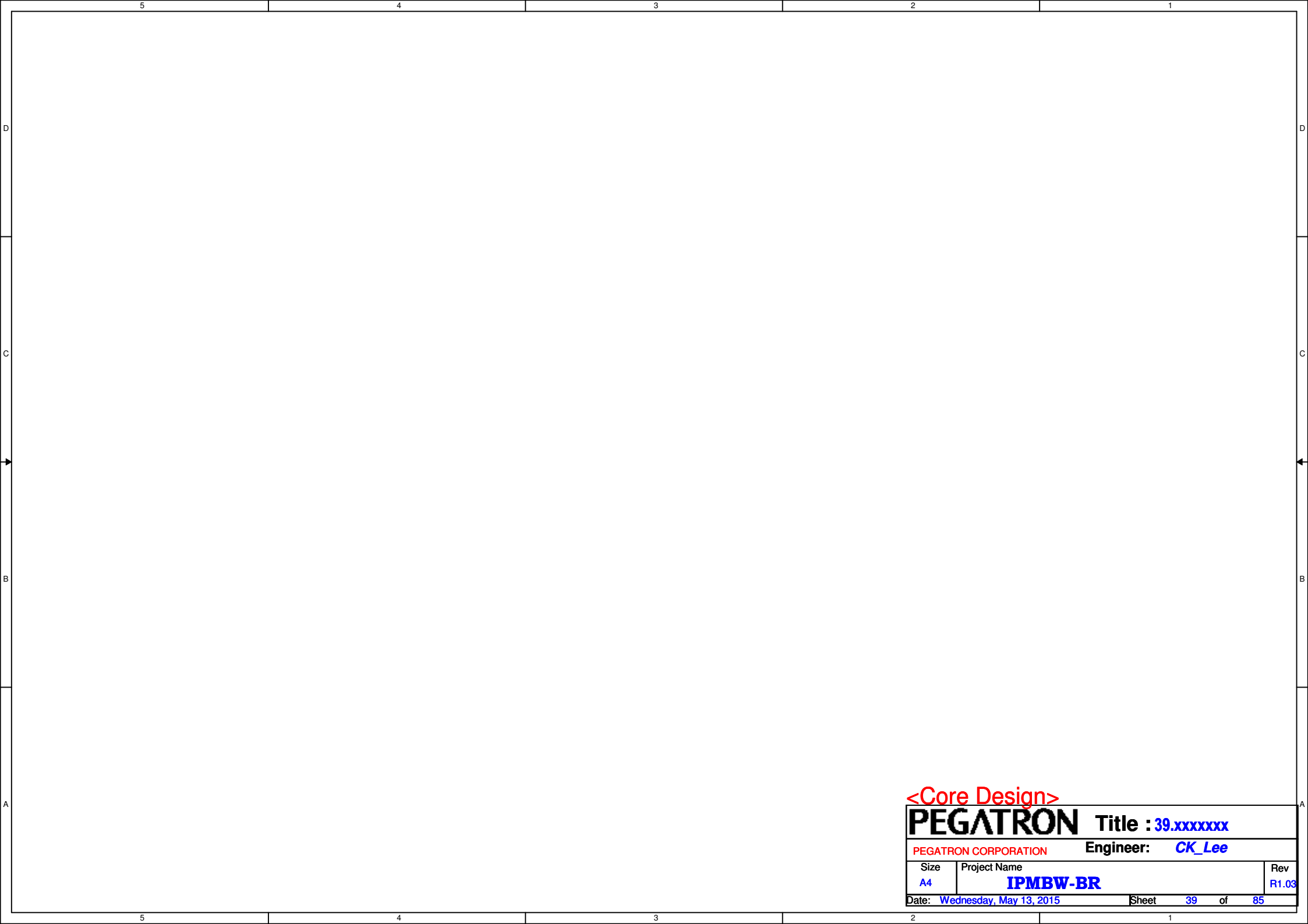


<Core Design>

PEGATRON		Title : 37.EC ITE/8528-2	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size A4	Project Name IPMBW-BR		Rev R1.03
Date: Wednesday, May 13, 2015	Sheet	37	of 85

KB/MS Dongle





<Core Design>

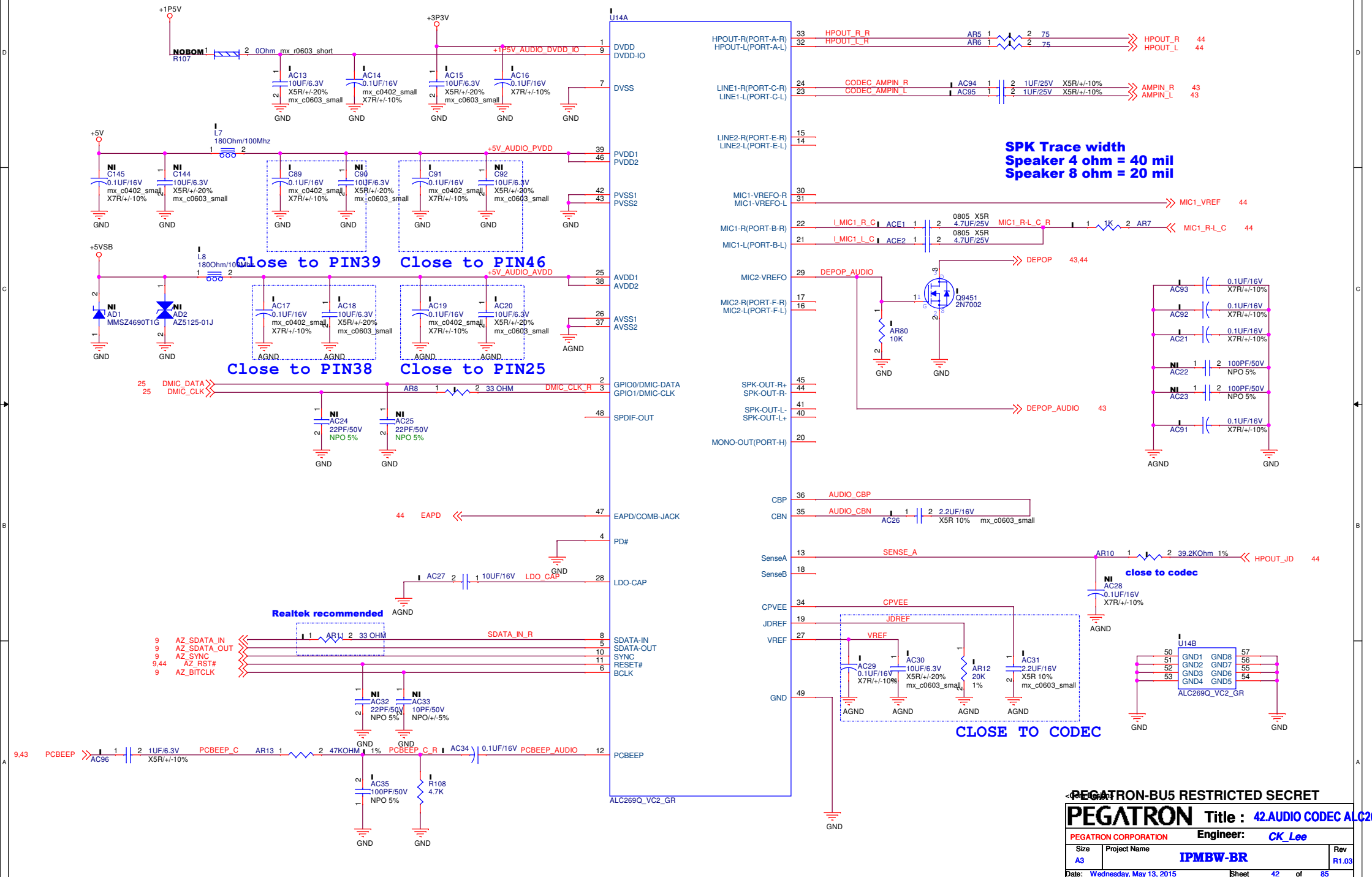
PEGATRON Title : 39.xxxxxxx

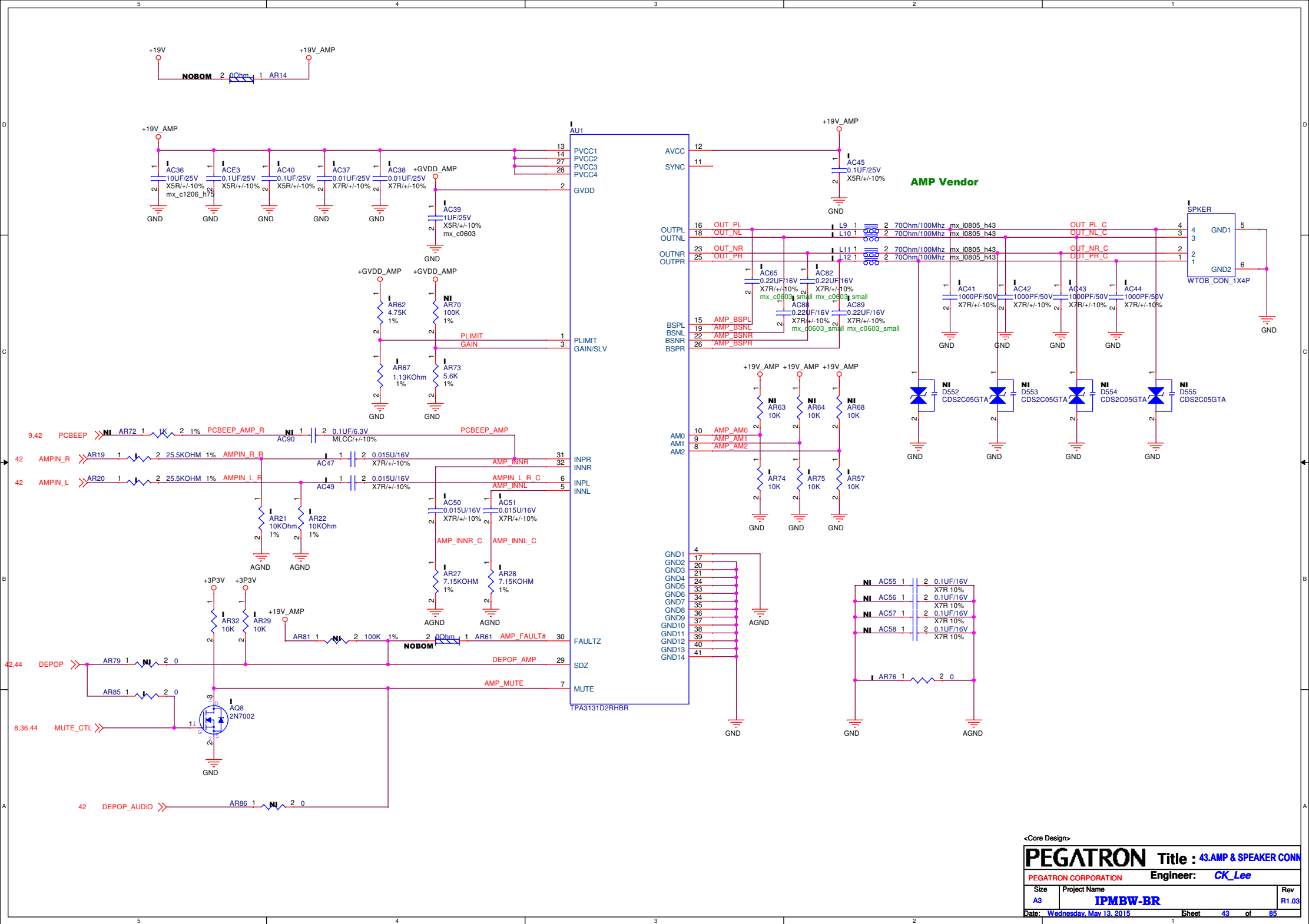
PEGATRON CORPORATION Engineer: CK_Lee

Size	Project Name	Rev
A4	IPMBW-BR	R1.03

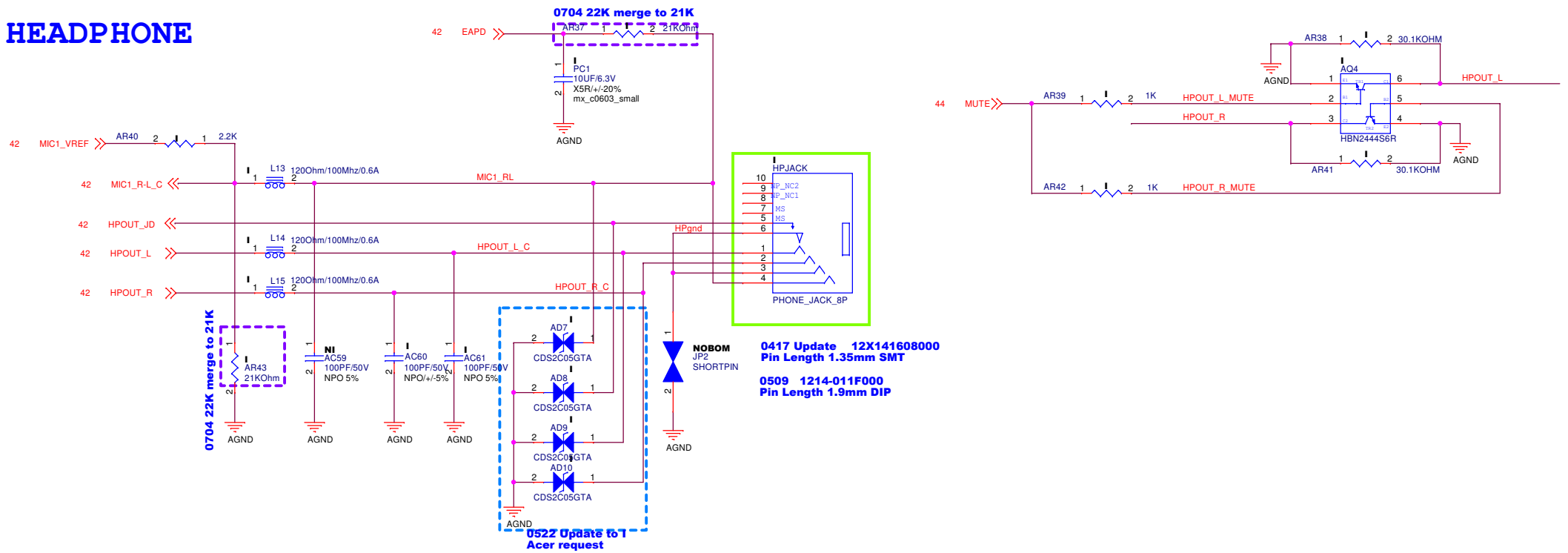
Date: Wednesday, May 13, 2015 Sheet 39 of 85

ALC269 CODEC

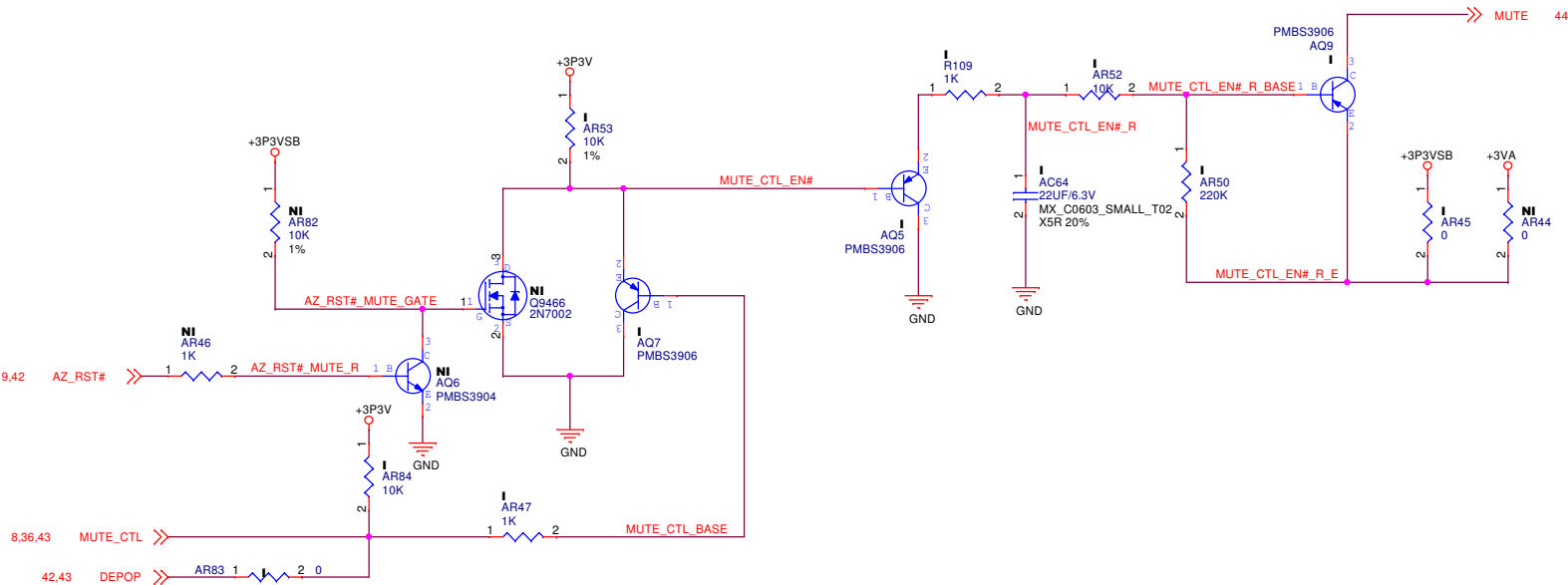




HEADPHONE



Audio MUTE



PCB1
PCB_BOARD

IPMBW-BR
PCB
Proprietary

SN_LABEL
42X7_WHITE

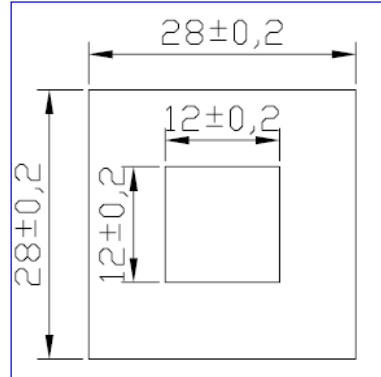
PPIDL8
PPID label

AMP
AMIL8
AMI label

BPLATE
BACK PLATE

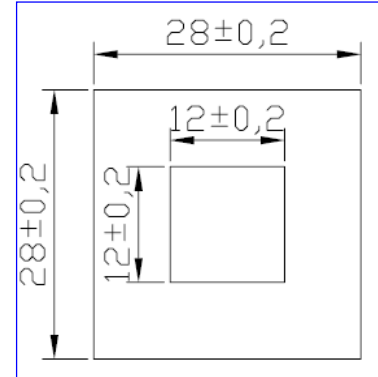
IPMBW-BR
BACK PLATE

MYLAR1



J1008607

GPU
MYLAR2



J1008607

<Core Design>

PEGATRON

Title : 45. PCB & Label & Mylar

PEGATRON CORPORATION

Engineer: CK_Lee

Size
A3

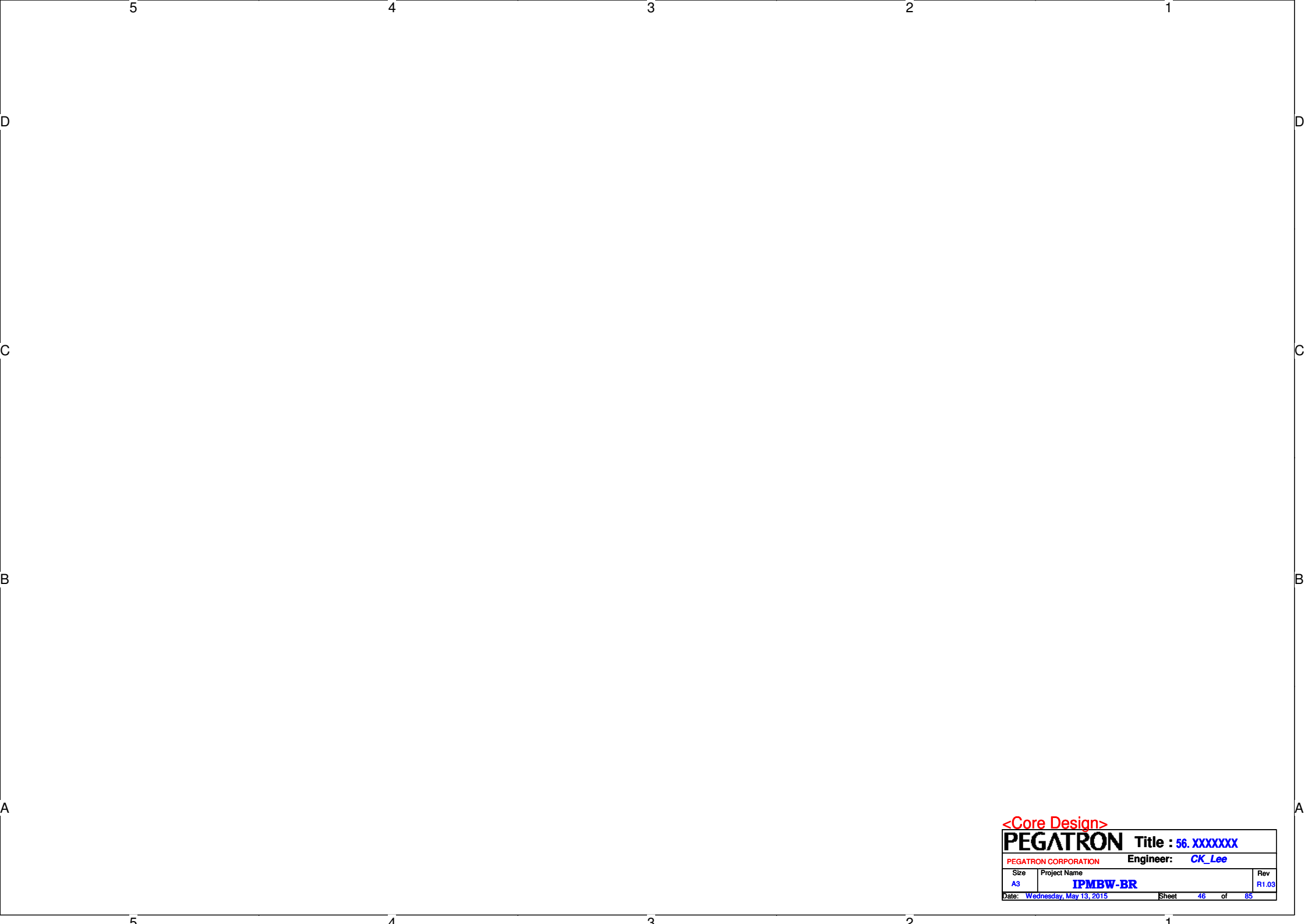
Project Name

IPMBW-BR

Rev
R1.03

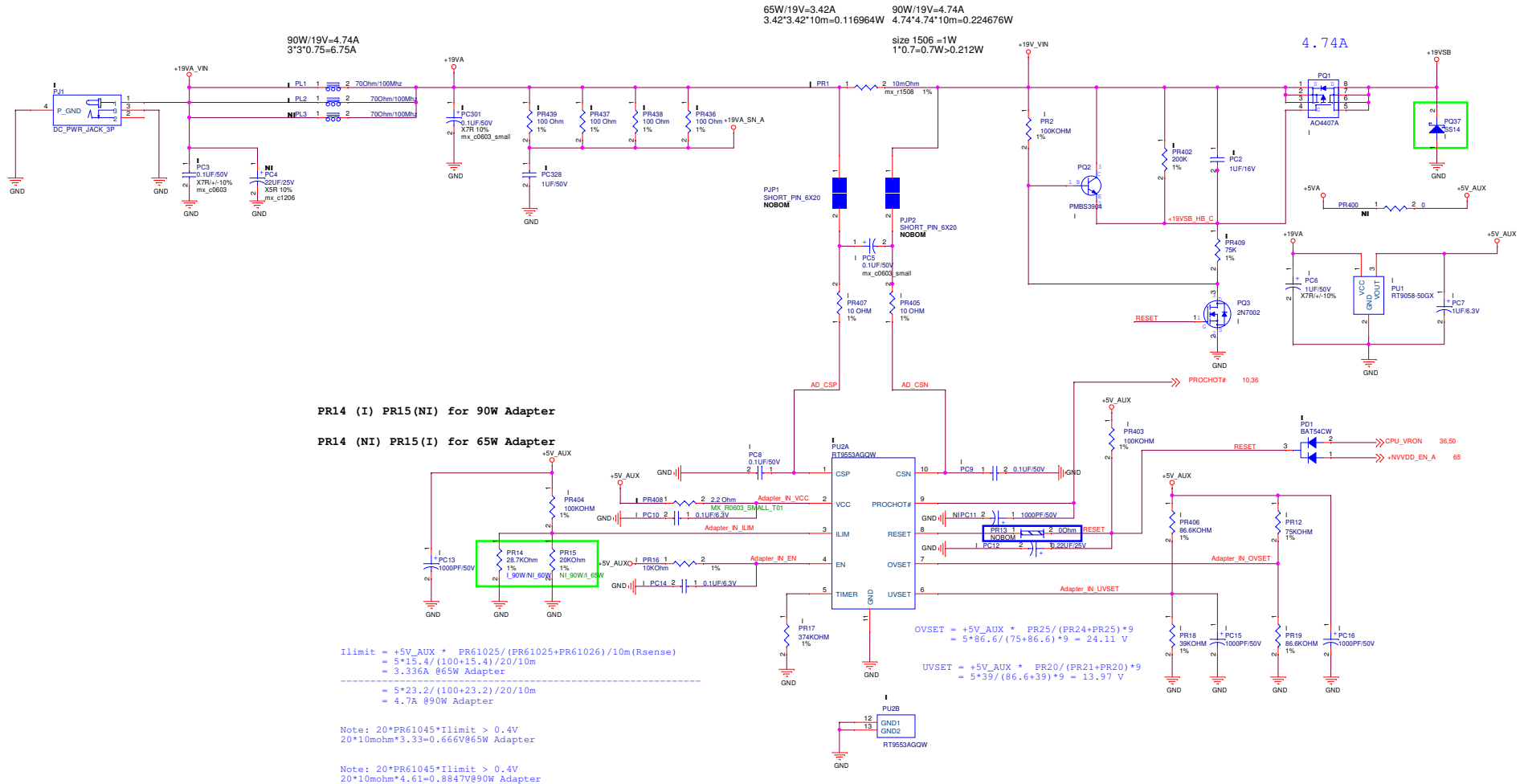
Date: Wednesday, May 13, 2015

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<Core Design>

PEGATRON		Title : 56. XXXXXX	
PEGATRON CORPORATION		Engineer: CK_Lee	
Size A3	Project Name IPMBW-BR		Rev R1.03
Date: Wednesday, May 13, 2015		Sheet	46 of 85



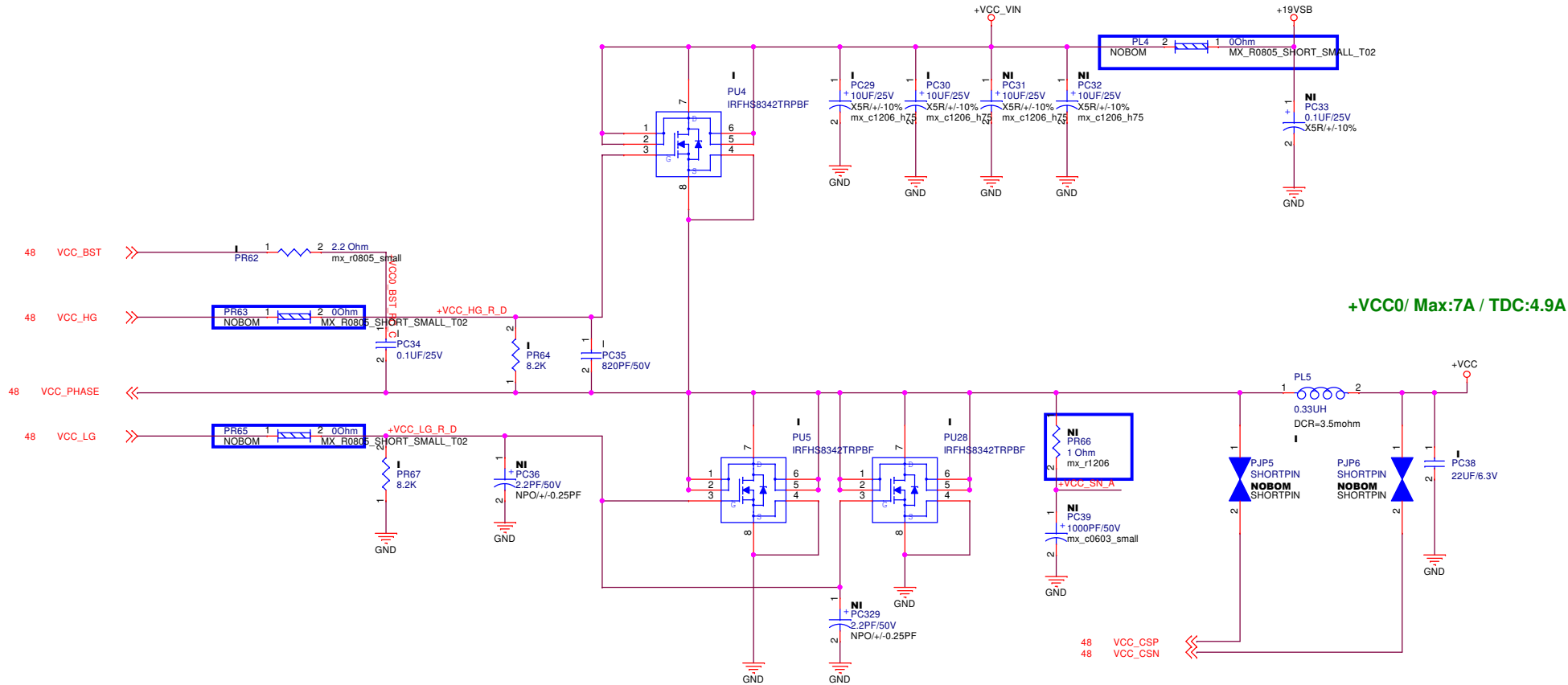
<Core Design>			
File	<Title>		
Size	Document Number	Rev	
AC	PM4W-SR	P1.0	
Date:	Wednesday, May 13, 2015	Sheet	47 of 85

+VCC, PLACE NEAR CPU

$I_{in}=0.53A$

Fsw=500kHz
 $I_{in}=0.29934$
 $I_{n,rms}=$
 $ripple=2.37A$
 $H/S=0.227W$
 $L/S=0.793W$
 $OCP=14.5$

EFF=57.97%@10%Imax
 EFF=81.38%@TDC
 EFF=79.99%@Imax

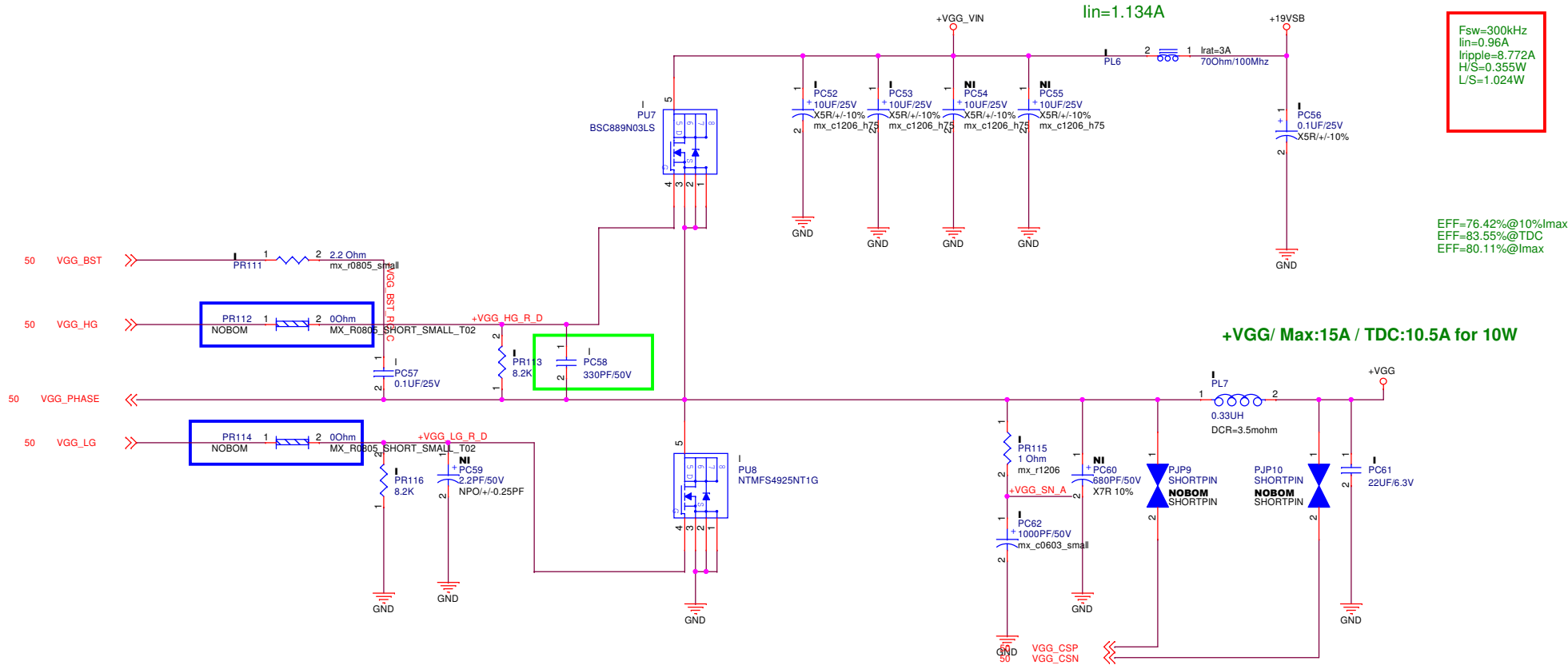


Owner	Worst case	Low Limit	High Limit
zIVO	14A	TBD	32A
ChenYang			

<Core Design>

Title		Rev
<Title>		R1.09
Size A3	Document Number IPMBW-BR	
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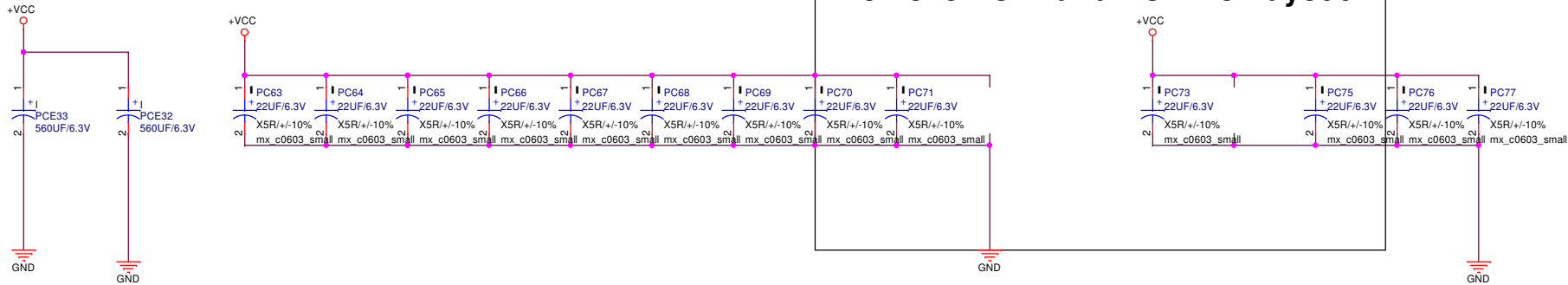
+VGG, PLACE NEAR CPU



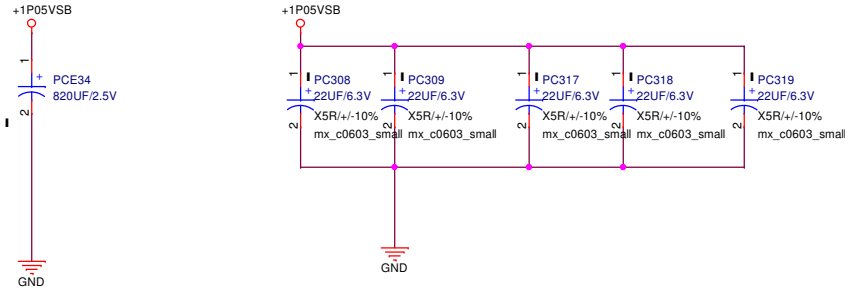
Owner	Worst case	Low Limit	High Limit
ZIVO	22.5A	TBD	32A
ChenYang			

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Size	Document Number	Rev
A3	IPMBW-BR	R1.08
Date:	Wednesday, May 13, 2015	Sheet 51 of 85

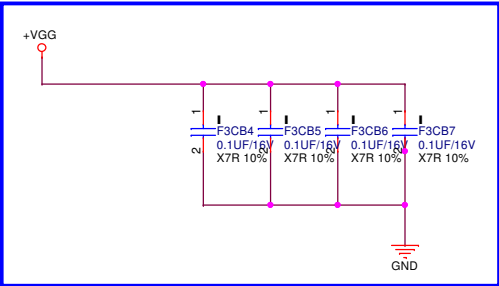
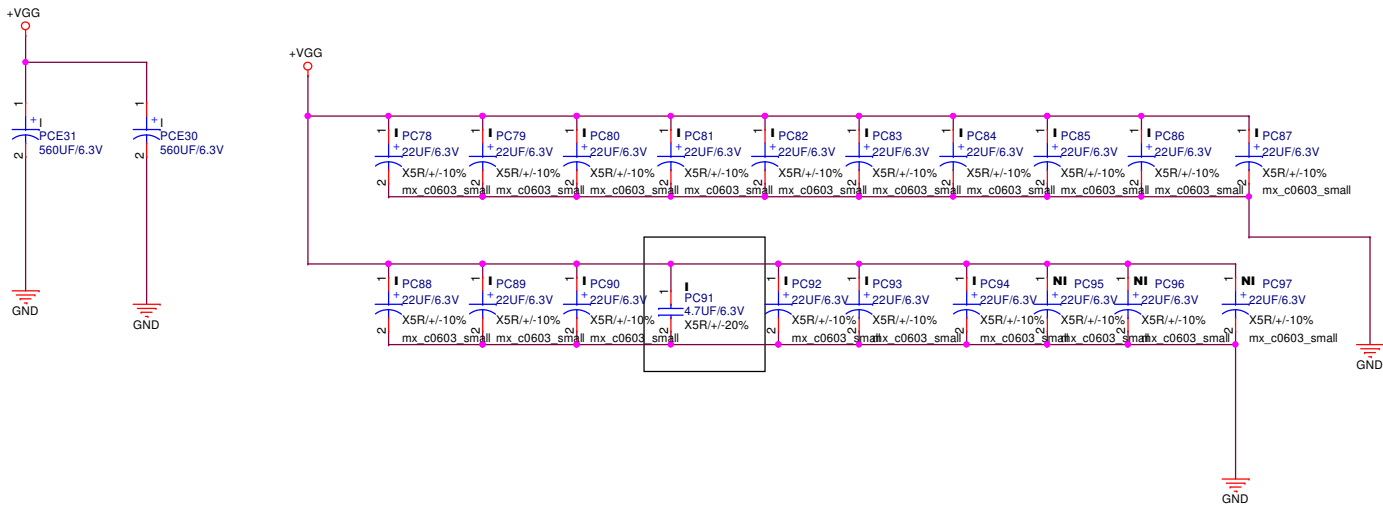
+VCC0 Output CAP



+VNN Output CAP

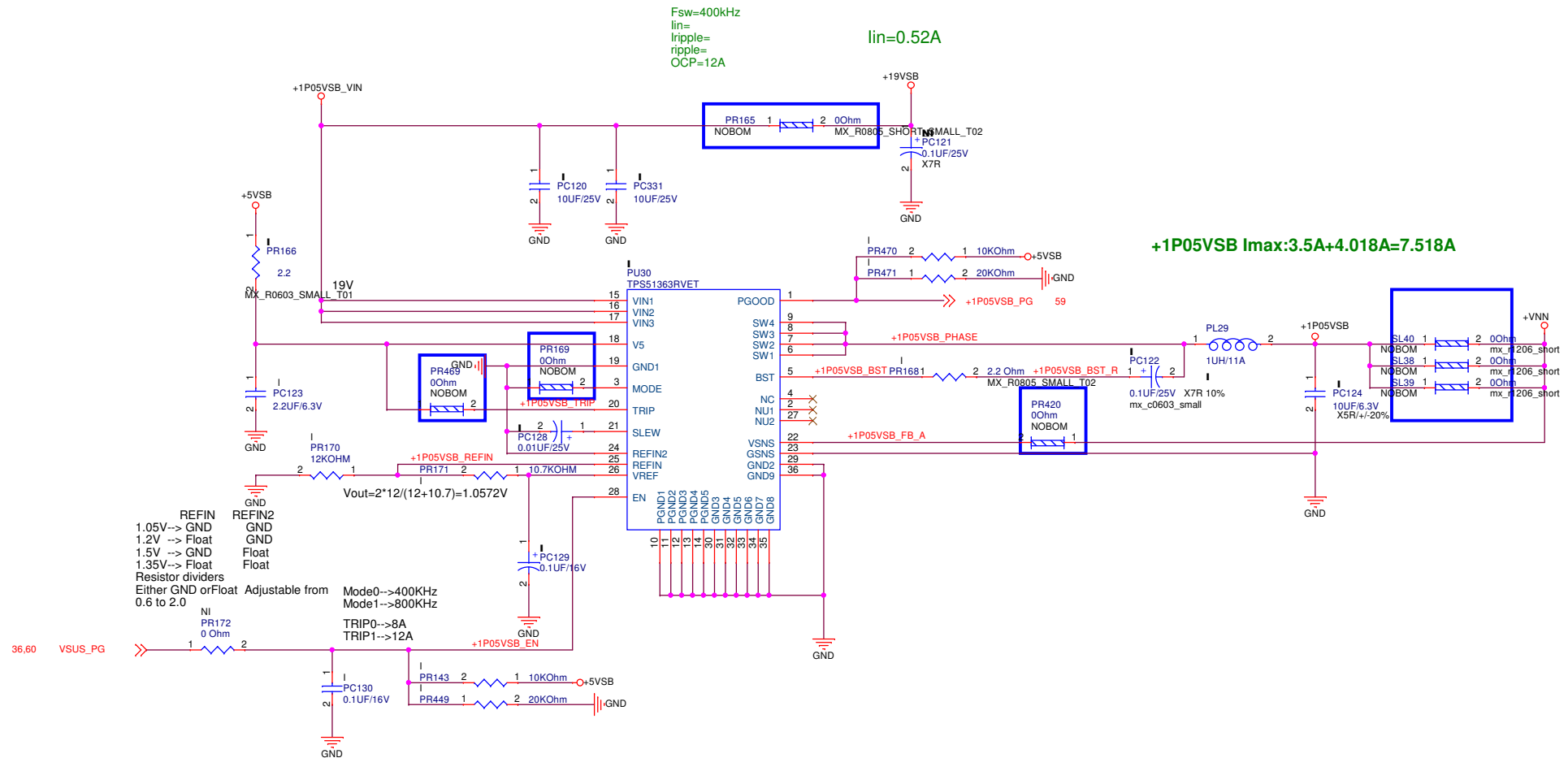


+VGG Output CAP



Cross Moart Cap

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A3	IPMBW-BR		R1.0b
Date:	Wednesday, May 13, 2015	Sheet	52 of 85

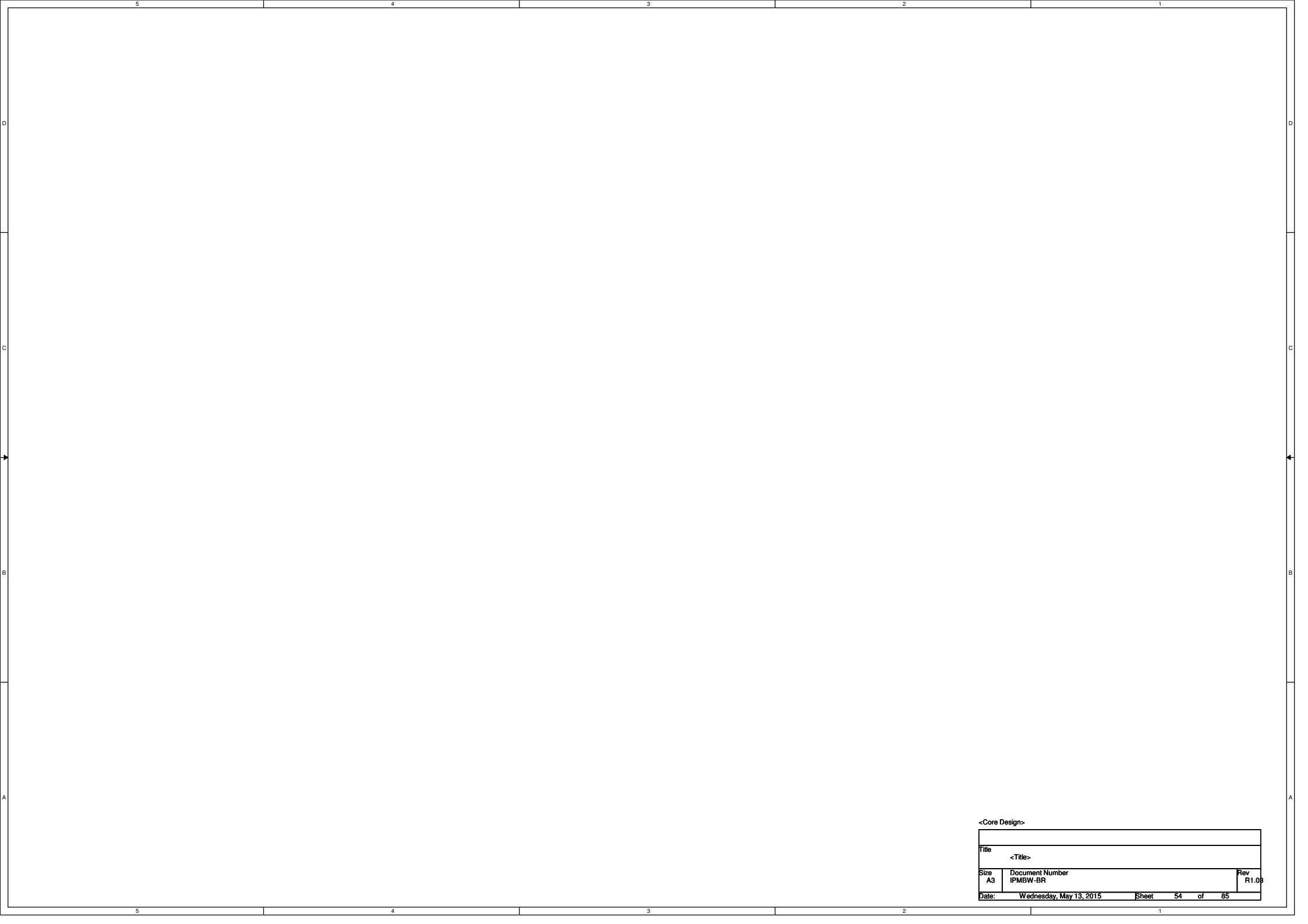


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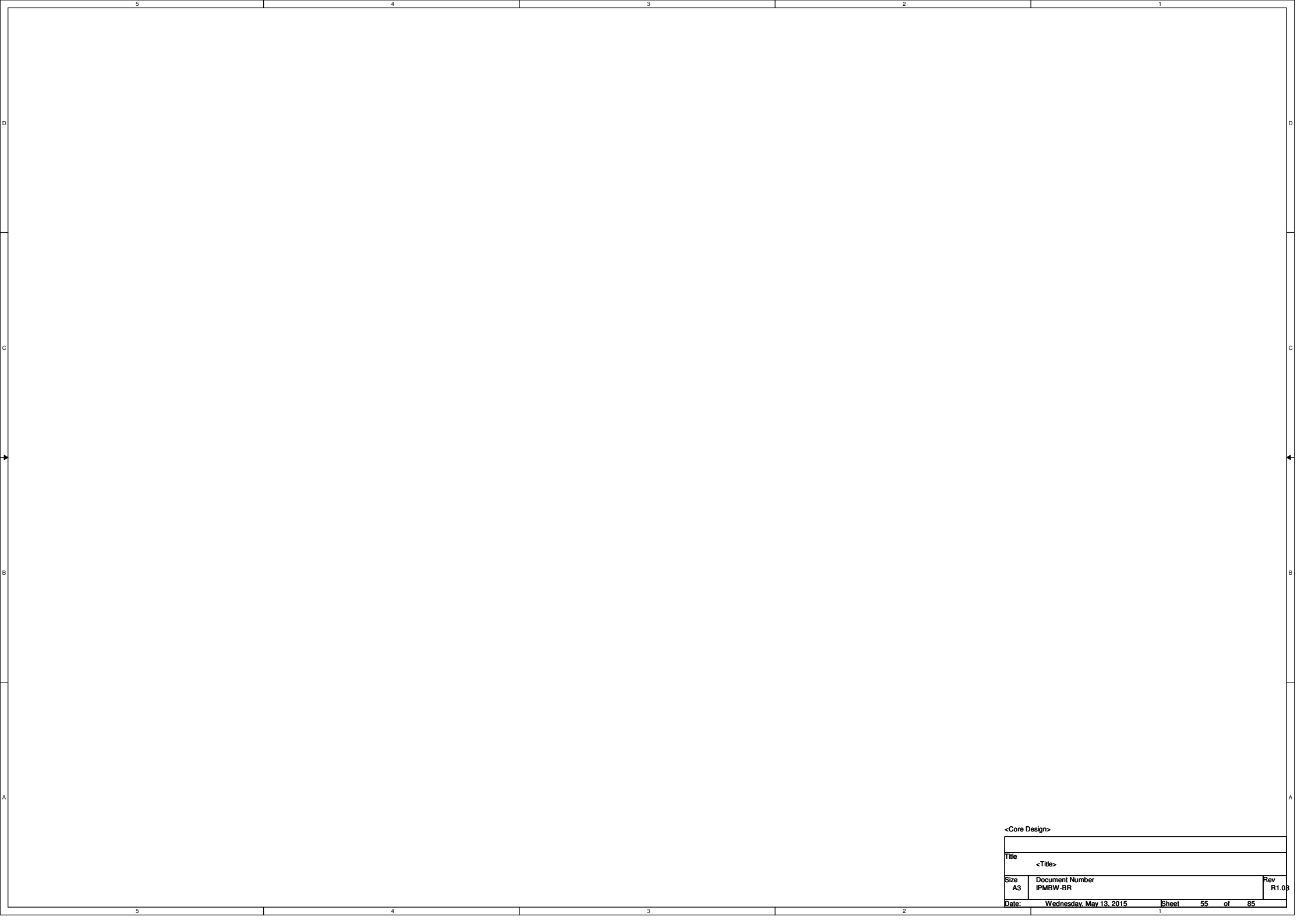
PEGATRON Title : +1P05VSB

PEGATRON CORPORATION Engineer: CK_Lee

Size	Project Name	Rev
A3	IPMBW-BR	R1.03
Date: Wednesday, May 13, 2015	Sheet 53 of 85	

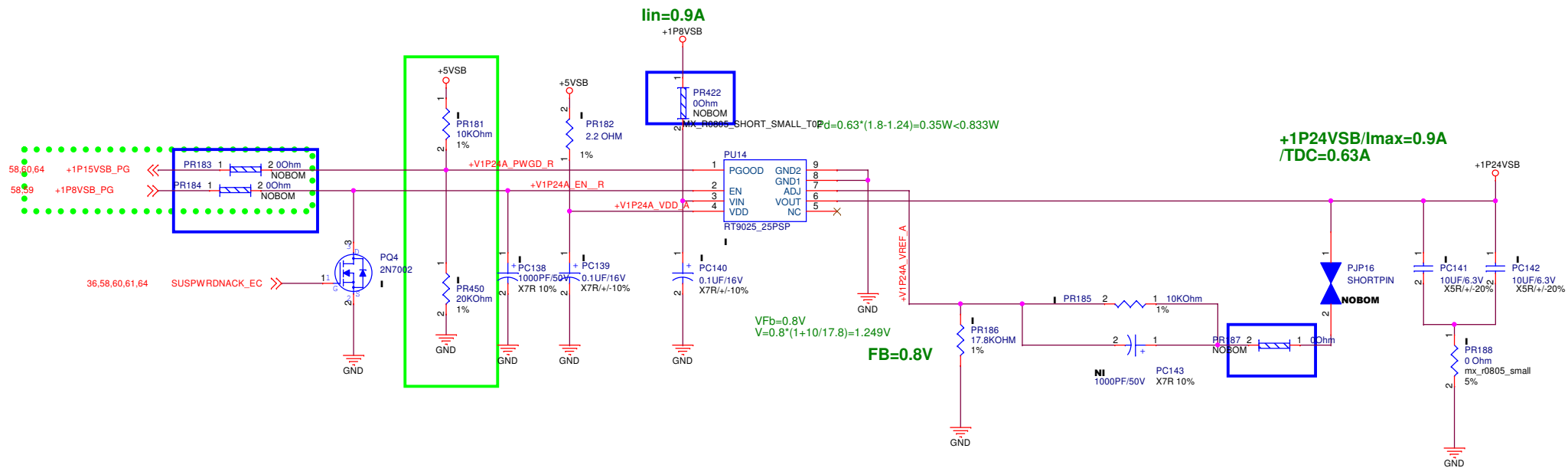


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Size	Document Number		
A3	IPMBW-BR		
Rev			R1.00
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Size	Document Number		Rev
A3	IPMBW-BR		R1.09
Date:	Wednesday, May 13, 2015		Sheet 55 of 85



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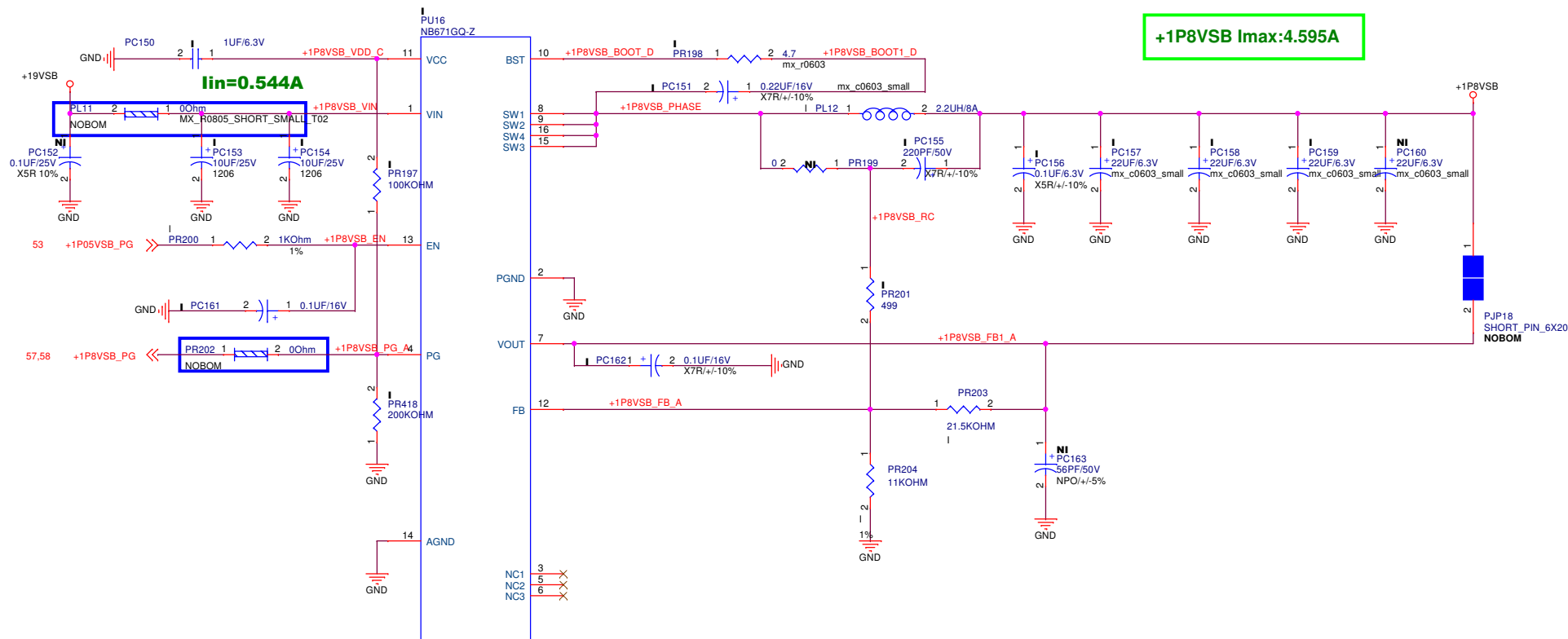
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Document Number
IPMBW-BR

Rev
R1.00

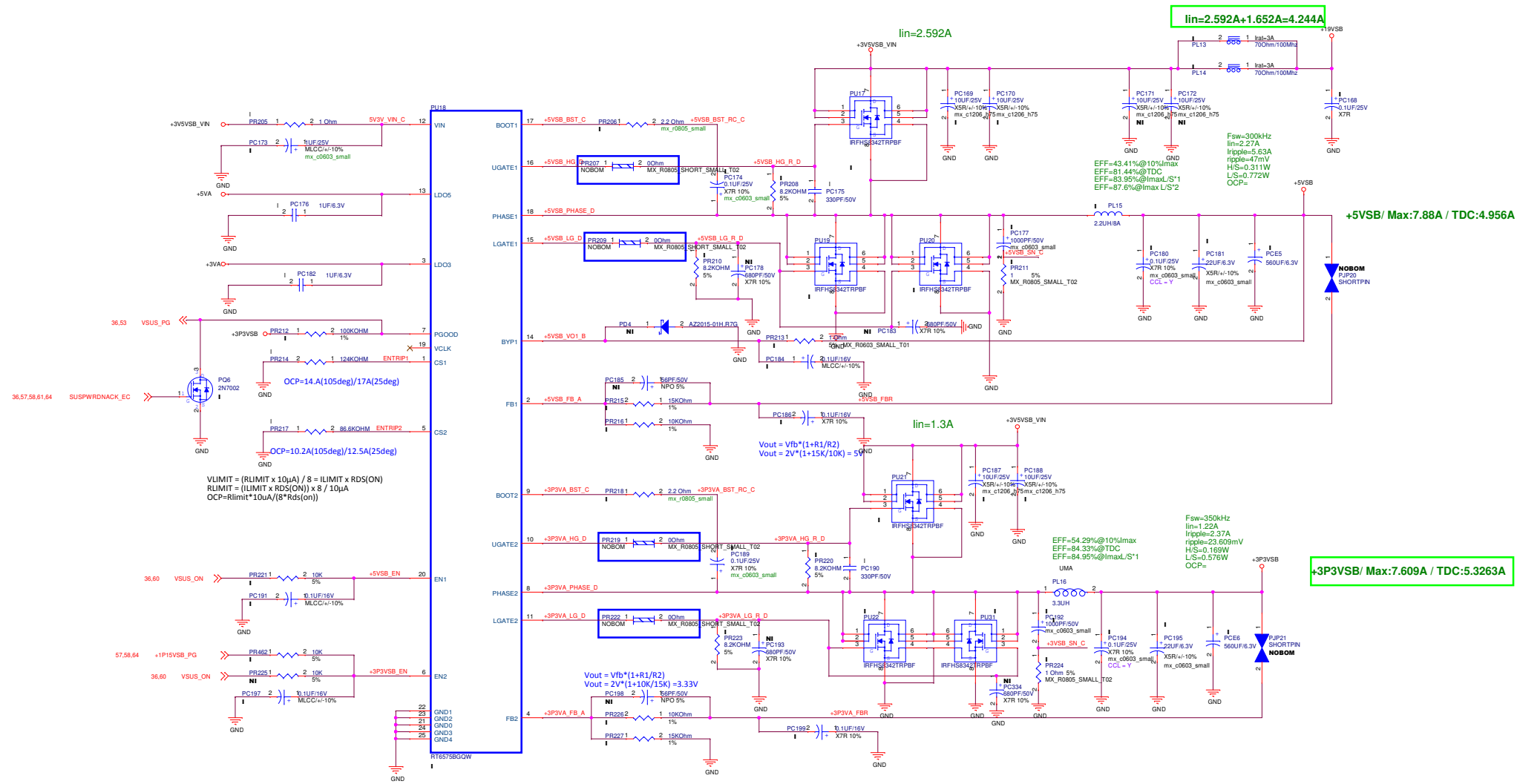
Date: Wednesday, May 13, 2015

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Title		
<Title>		
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$V_{LIMIT} = (R_{LIMIT} \times I_{LIMIT}) / 8 = I_{LIMIT} \times R_{DS(ON)}$
 $R_{LIMIT} = (I_{LIMIT} \times R_{DS(ON)}) \times 8 / I_{LIMIT}$
 $OCP = R_{LIMIT} \times I_{LIMIT} / (8 \times R_{DS(ON)})$

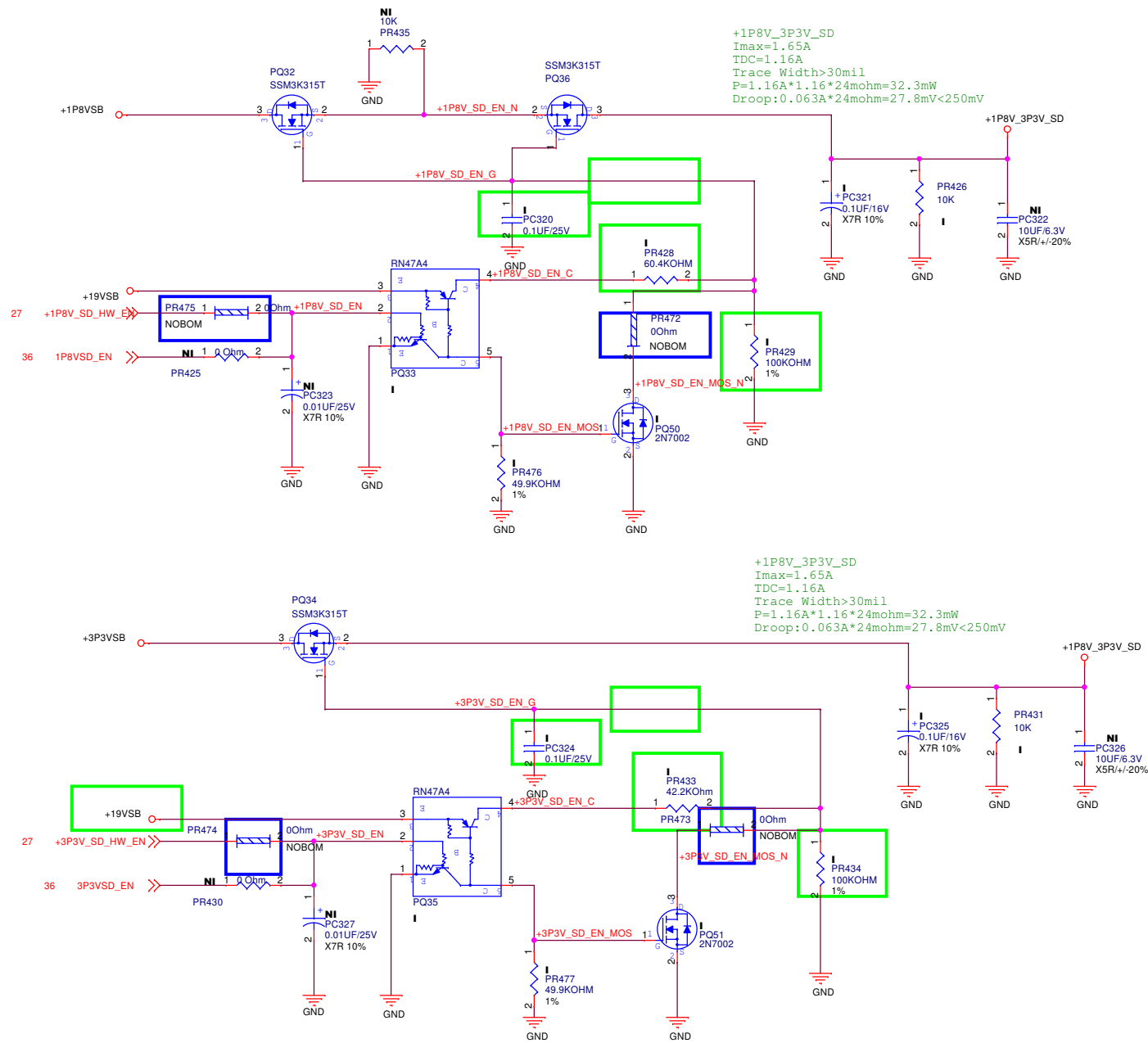
$OCP = 14.5A(105deg)/17A(25deg)$
 $OCP = 10.2A(105deg)/12.5A(25deg)$

$I_{in} = 2.592A + 1.652A = 4.244A$

+5VSB/ Max:7.88A / TDC:4.956A

+3P3VSB/ Max:7.609A / TDC:5.3263A

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Size			
AC	Document Number	Rev	R1.0
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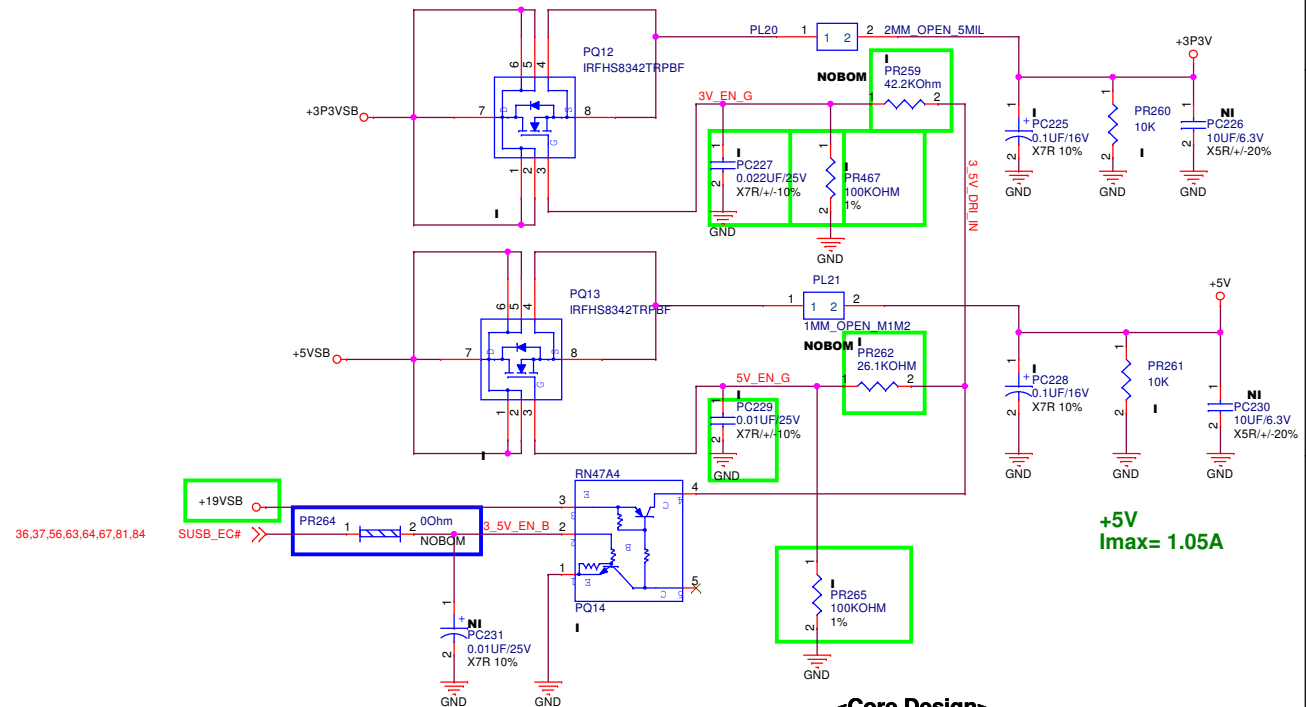
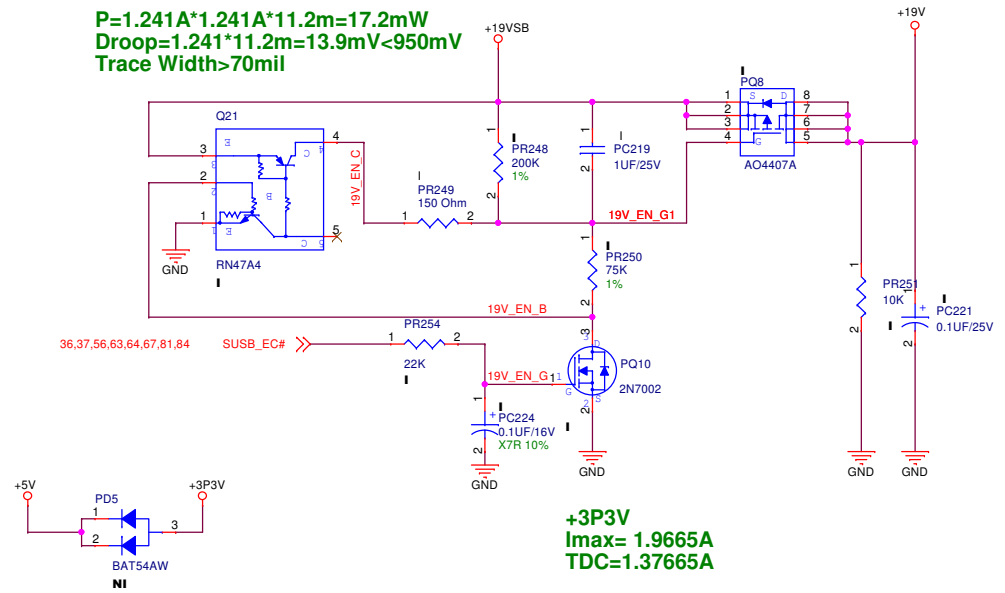


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+19VSB ==> +19V
I_{max}= ??A

$P=1.241A \times 1.241A \times 11.2m=17.2mW$
 $\text{Droop}=1.241 \times 11.2m=13.9mV < 950mV$
 Trace Width > 70mil

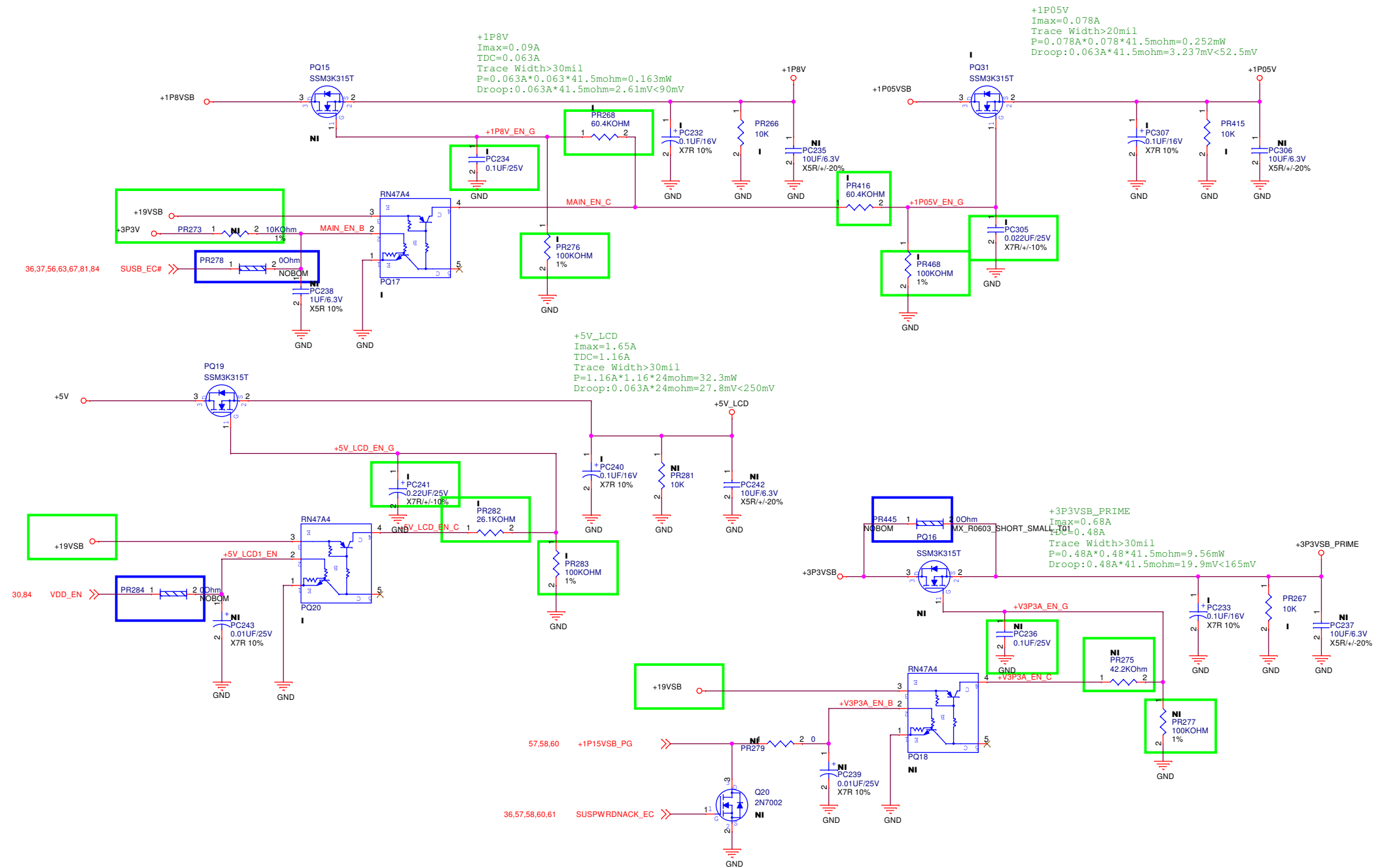


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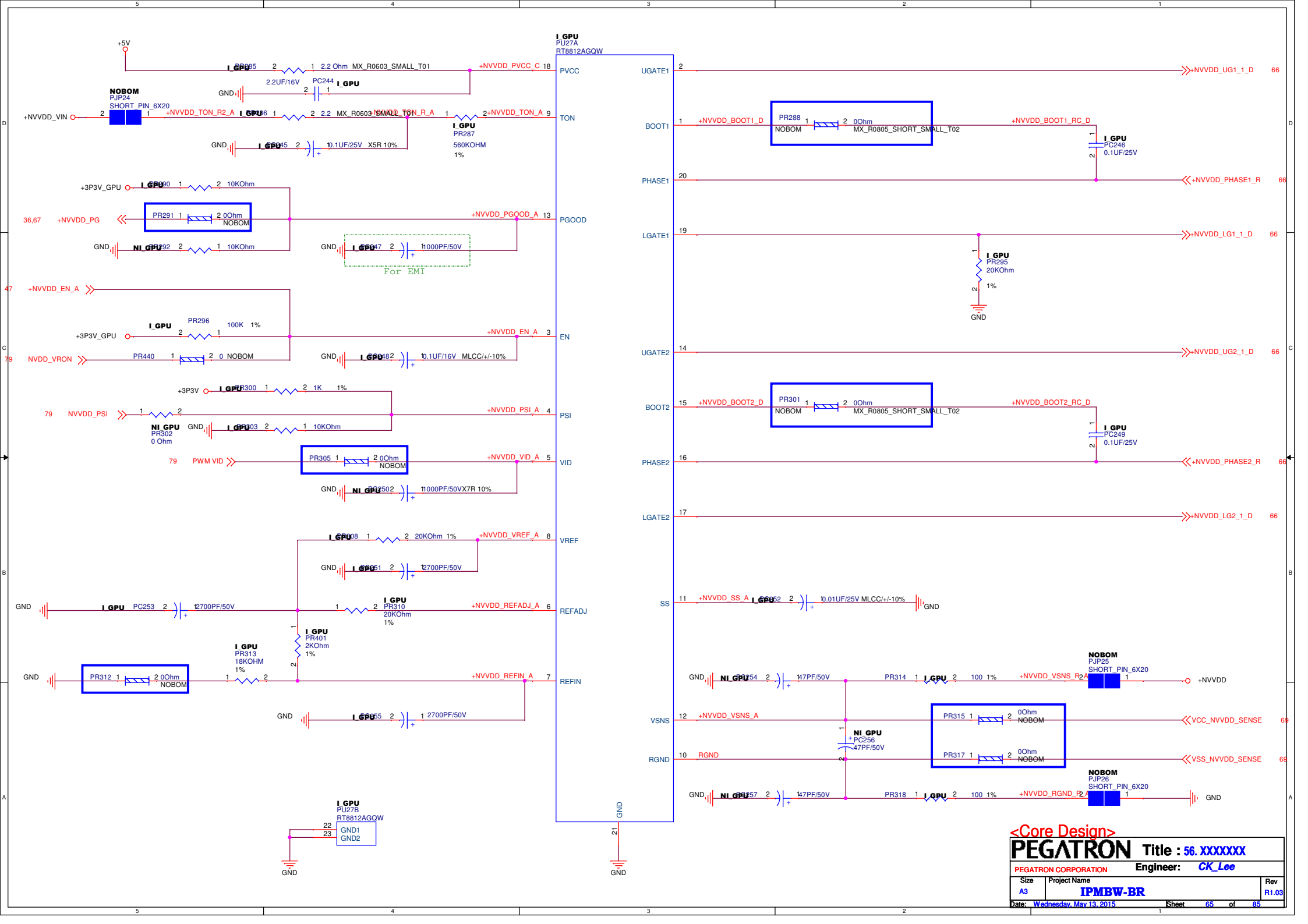
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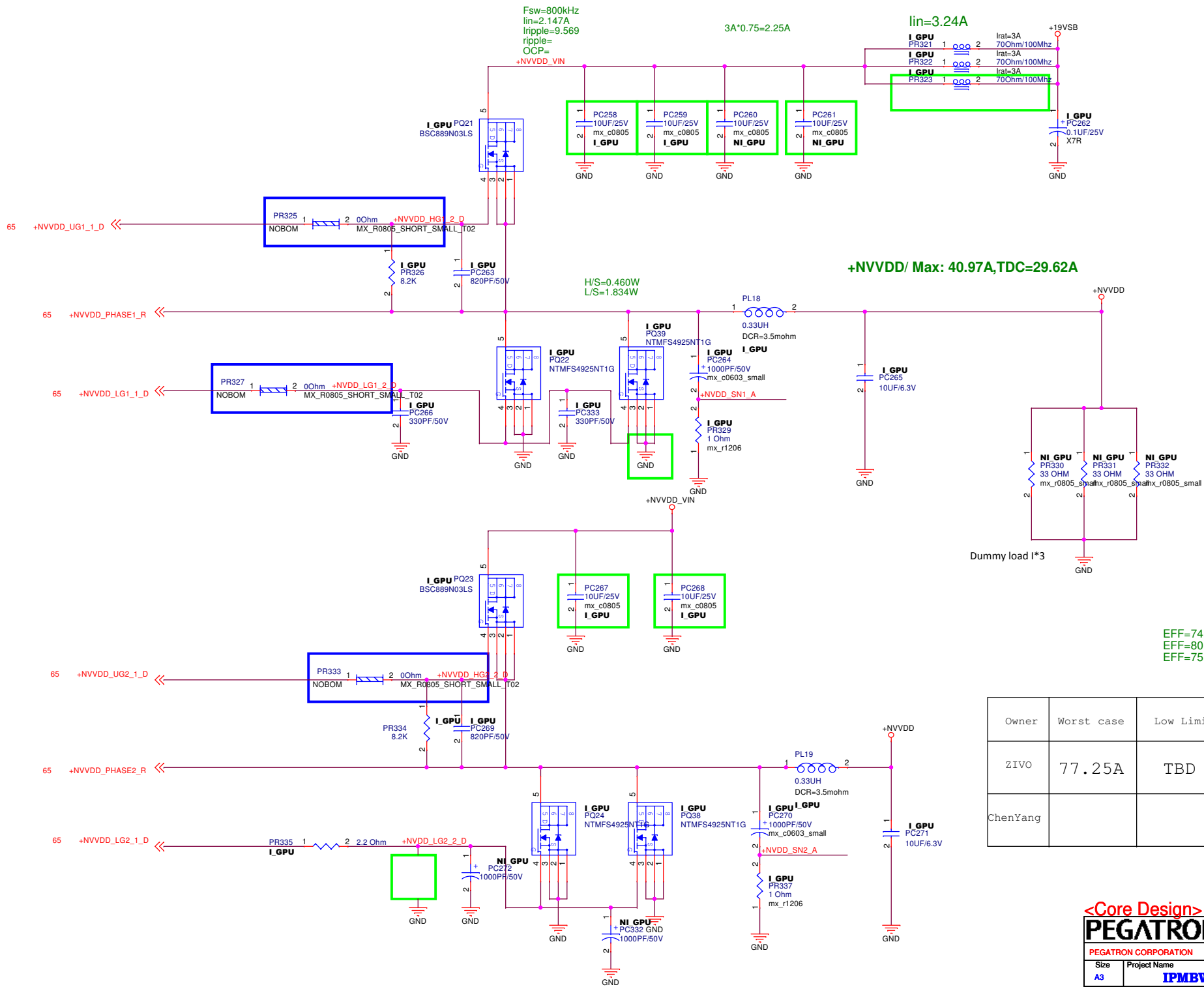
PEGATRON CORPORATION Engineer: CK_Lee

Size	Project Name	Rev
A3	IPMBW-BR	R1.03
Date: Wednesday, May 13, 2015	Sheet 63 of 85	

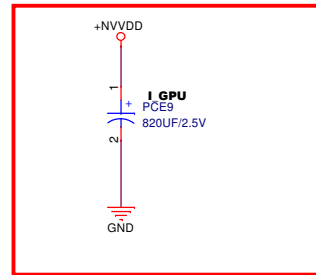


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Size	Document Number	Rev
A3	IPMBW-BR	R1.09
Date:	Wednesday, May 13, 2015	Sheet 64 of 85

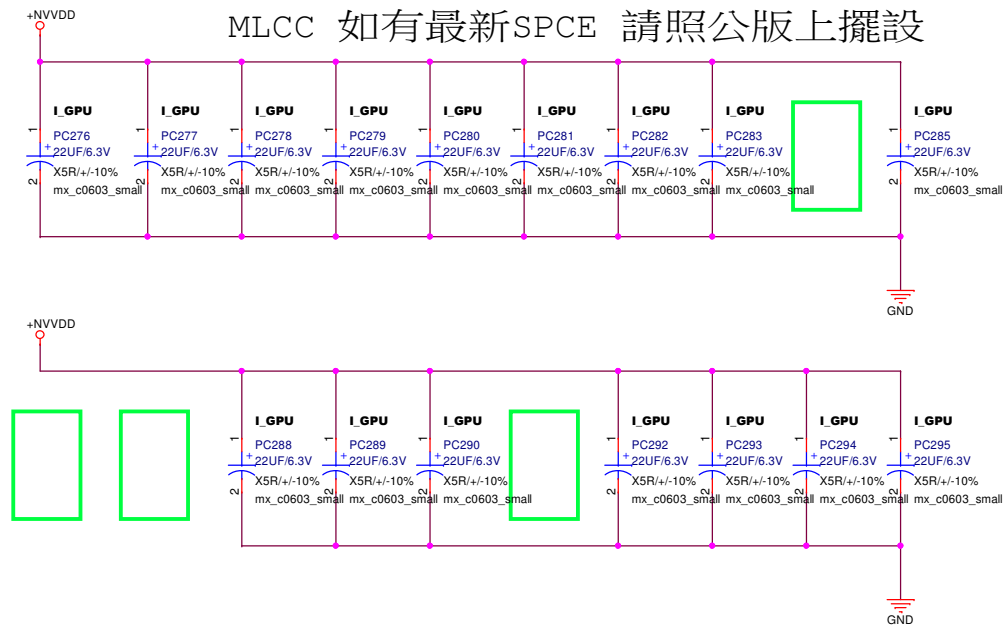




Power VR 輸出端



MLCC 如有最新SPCE 請照公版上擺設



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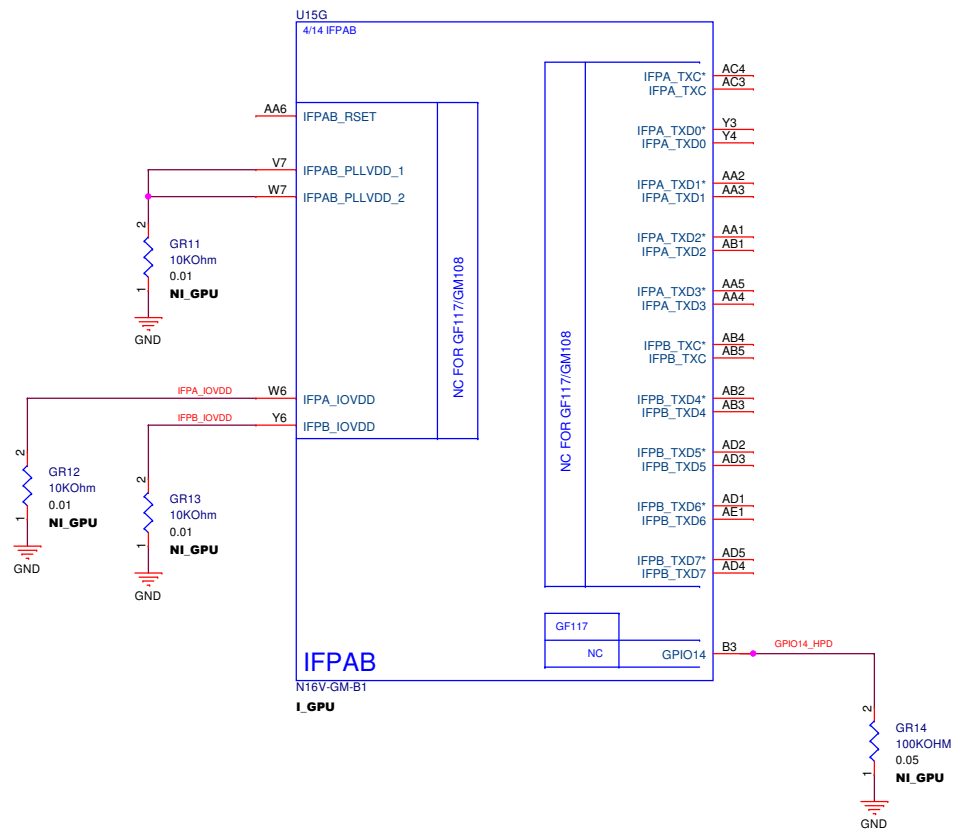
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PEGATRON CORPORATION Engineer: CK_Lee

Size A3	Project Name IPMBW-BR	Rev R1.03
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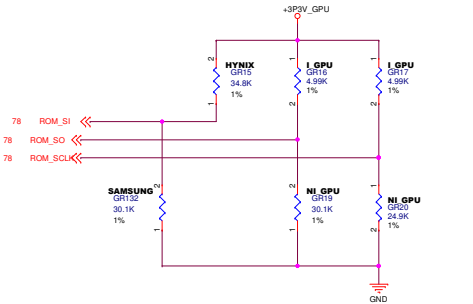
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IFPA/B LVDS Dual Link



Straps Mapping

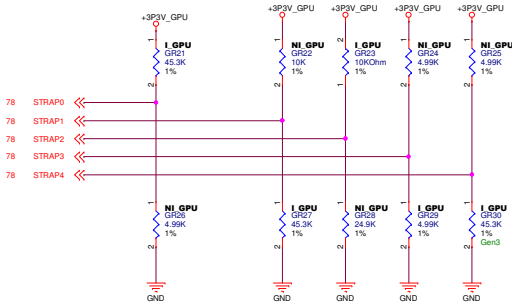
Will need to check and follow the update in PUN									
N16V-GM-S DID0x1299 10011001									
	ROM_SCL	1	1	0	0	PU	24.9Kohm	1%	
		0(No Video BIOS ROM)					4.99Kohm	1%	
	ROM_SI	1	1	1	0 0xE	PU	34.8Kohm	1%	
		0	0	1	0x5	PD	30.1Kohm	1%	
	ROM_SO	1	0	0	0	PU	4.99Kohm	1%	
	STRAP0	1	1	1	1	PU	45.3Kohm	1%	
	STRAP1	0	1	1	1	PD	45.3Kohm	1%	
	STRAP2	1	0	0	1	PU	10Kohm	1%	
	STRAP3	0	0	0	0	PD	4.99Kohm	1%	
	STRAP4	0	1	1	1	PD	45.3Kohm	1%	



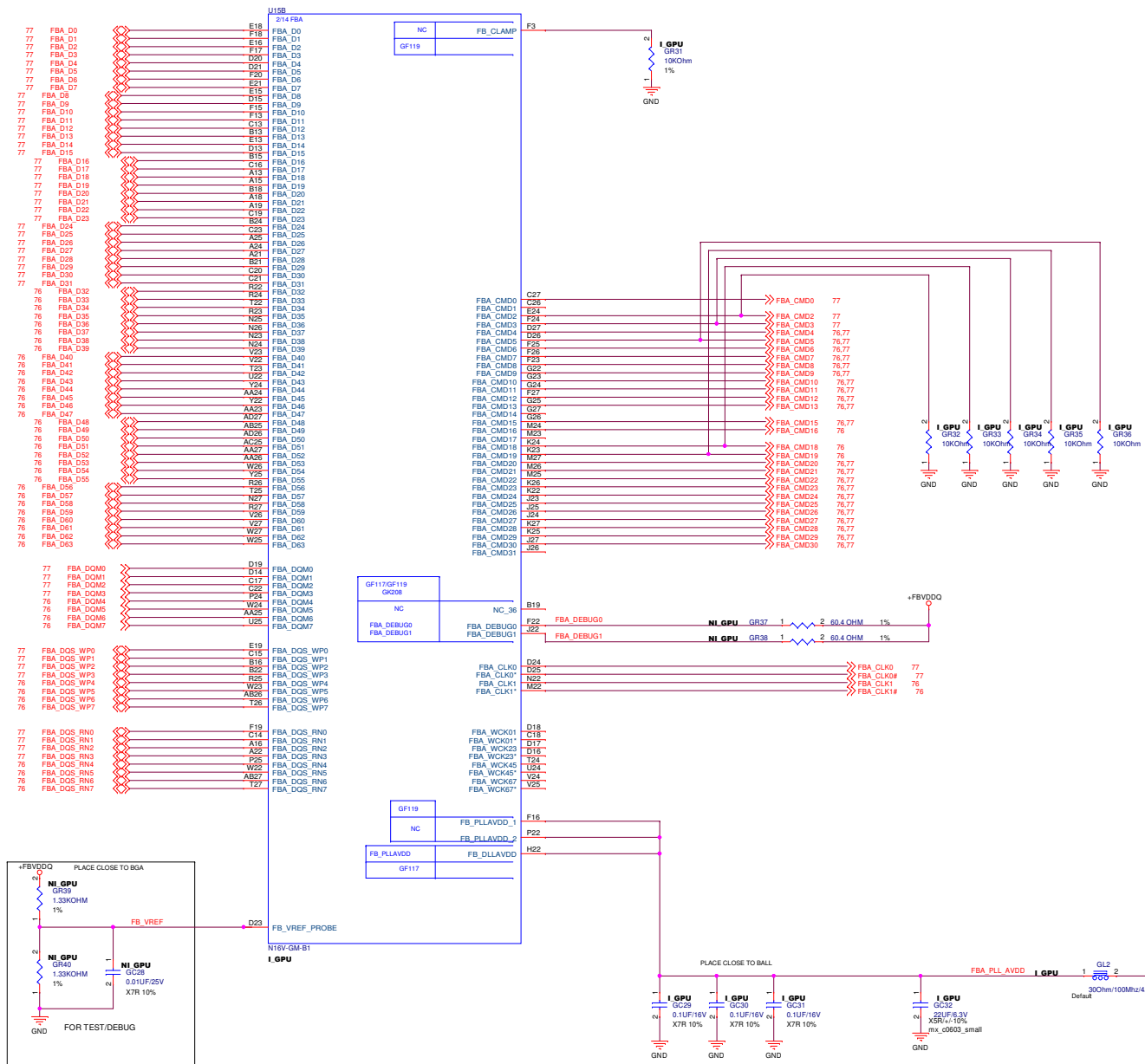
Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0	Resistor Values	Pull-up to VDD33	Pull-down to GND
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	4.99 kΩ	1000	0000
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	10.0 kΩ	1001	0001
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	15.0 kΩ	1010	0010
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	20.0 kΩ	1011	0011
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	24.9 kΩ	1100	0100
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	30.1 kΩ	1101	0101
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	34.8 kΩ	1110	0110
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	45.3 kΩ	1111	0111

Table 2. N16V-GM DDR3L Recommended Memories

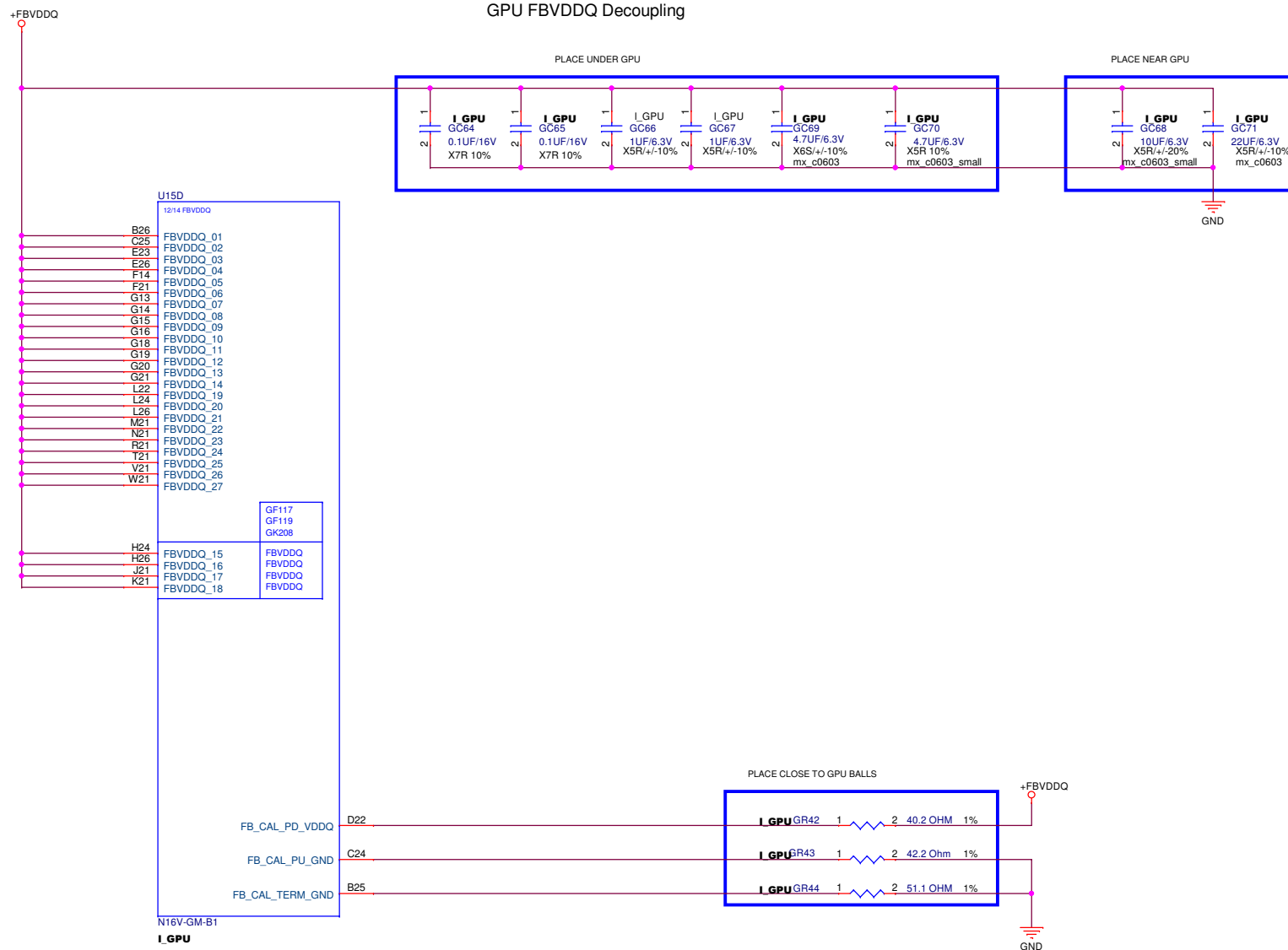
Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status	
DDR3L	1.35V/ 1.35V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63FR-11C	F-die	0x8	900	N/A	Production candidate	
				Micron	MT41J128M16JT-093G:K	K-die	0x8	900	1322	Production candidate	
				Samsung	K4VWQ1646Q-BC1A	Q-die	0x7	900	N/A	Production candidate	
		256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0xE	900	N/A	Production candidate	
				Micron	MT41J256M16HA-093G:E	E-die	0xD	900	1322	Production candidate	
				Samsung	K4V4G1646D-BC1A	D-die	0x5	900	N/A	Production candidate	
				Dual Rank	Hynix	H5TC4G63AFR-11E	A-die	0xE	900	N/A	Production candidate
					Micron	MT41J256M16HA-093G:E	E-die	0xD	900	1322	Production candidate
					Samsung	K4V4G1646D-BC1A	D-die	0x5	900	N/A	Production candidate



Frame Buffer Partitions A/B

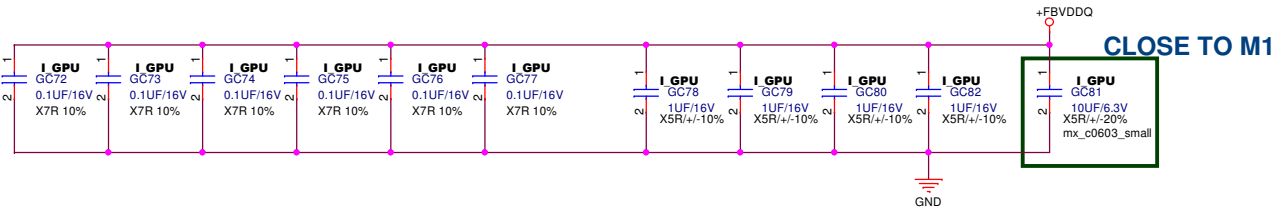


Frame Buffer FBVDDQ Power/Decoupling/Calibration

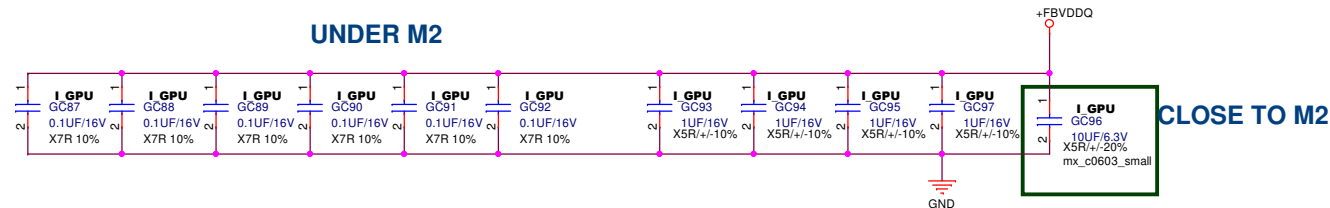


Memory FBVDD/Q Decoupling

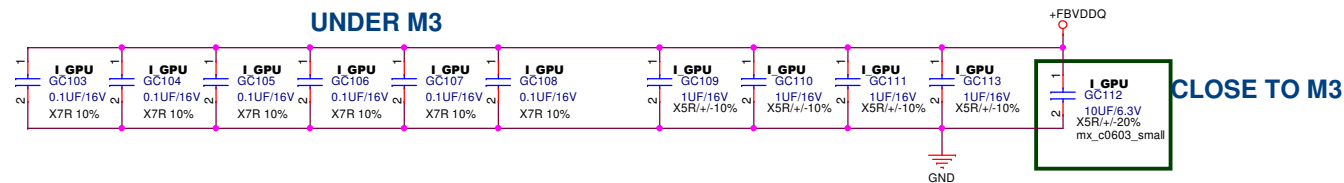
UNDER M1



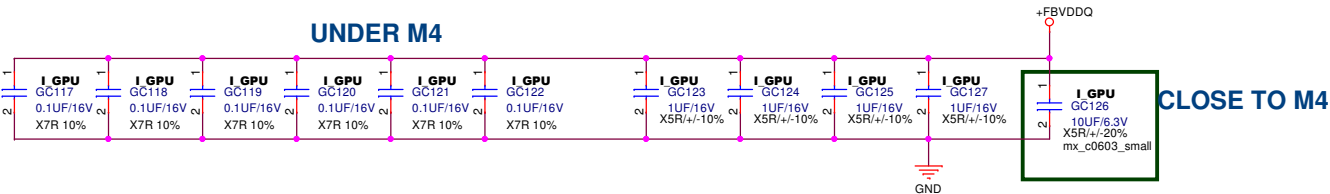
UNDER M2



UNDER M3



UNDER M4



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PEGATRON Title : 75.dGPU_Memory Decoupling

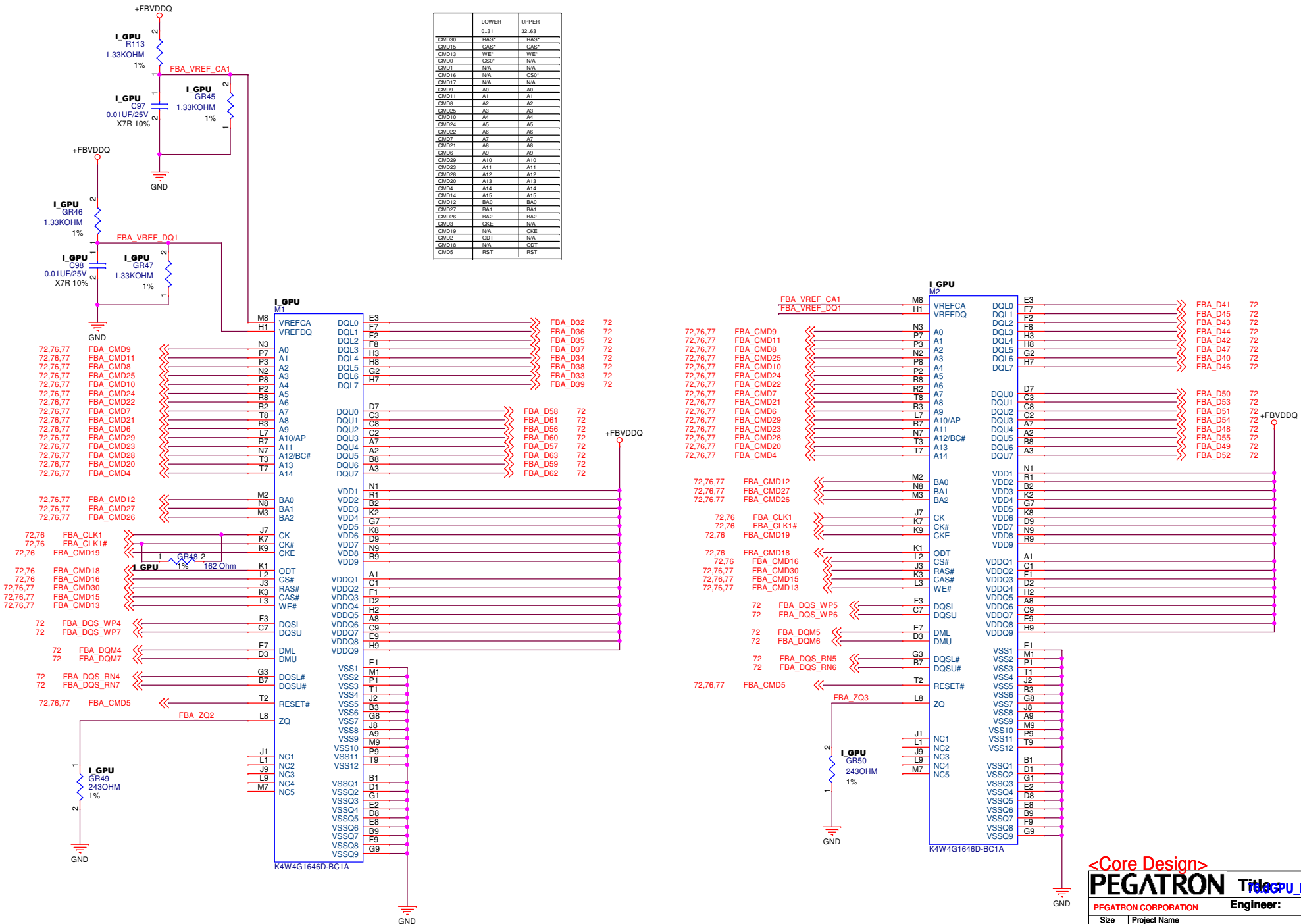
PEGATRON CORPORATION Engineer: CK_Lee

Size A3 Project Name IPMBW-BR Rev R1.03

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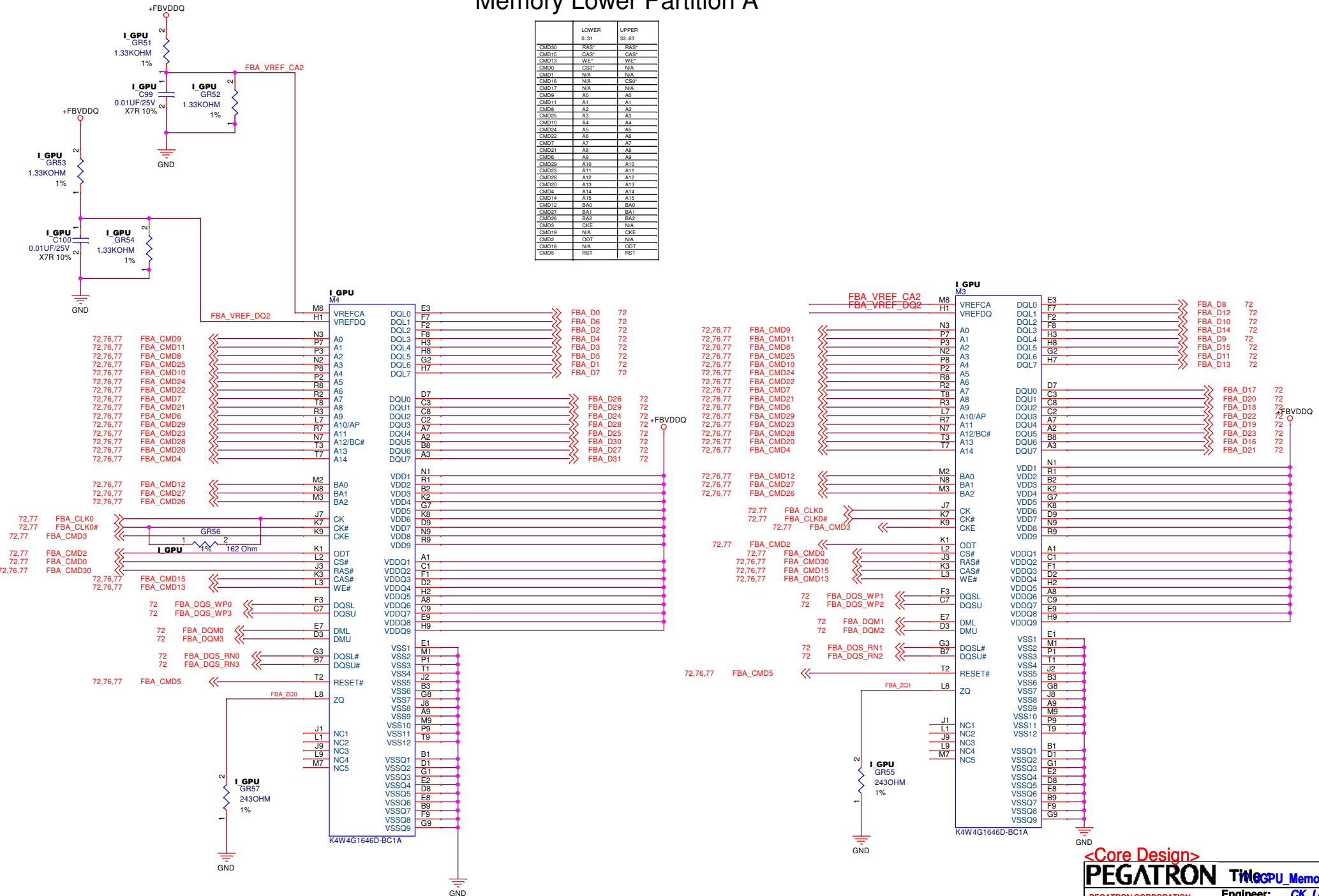
Memory Upper Partition A

	LOWER	UPPER
CM030	RAS*	RAS*
CM015	CAS*	CAS*
CM013	WE*	WE*
CM00	CS0*	N/A
CM01	N/A	N/A
CM016	N/A	CS0*
CM017	N/A	N/A
CM01	A0	A0
CM011	A1	A1
CM08	A2	A2
CM025	A3	A3
CM010	A4	A4
CM024	A5	A5
CM022	A6	A6
CM027	A7	A7
CM021	A8	A8
CM05	A9	A9
CM029	A10	A10
CM023	A11	A11
CM028	A12	A12
CM020	A13	A13
CM04	A14	A14
CM014	A15	A15
CM012	BA0	BA0
CM027	BA1	BA1
CM026	BA2	BA2
CM03	CKE	N/A
CM019	N/A	CKE
CM02	ODT	N/A
CM018	N/A	ODT
CM05	RST	RST



Memory Lower Partition A

	LOWER 0.31	UPPER 32.63
CMD30	RAS*	RAS*
CMD15	CAS*	CAS*
CMD13	WE*	WE*
CMD0	CS0*	N/A
CMD1	N/A	N/A
CMD16	N/A	CS0*
CMD17	N/A	N/A
CMD9	A0	A0
CMD11	A1	A1
CMD8	A2	A2
CMD25	A3	A3
CMD10	A4	A4
CMD24	A5	A5
CMD22	A6	A6
CMD7	A7	A7
CMD21	A8	A8
CMD6	A9	A9
CMD29	A10	A10
CMD23	A11	A11
CMD28	A12	A12
CMD29	A13	A13
CMD4	A14	A14
CMD14	A15	A15
CMD12	BA0	BA0
CMD21	BA1	BA1
CMD26	BA2	BA2
CMD3	CKE	N/A
CMD19	N/A	CKE
CMD2	ODT	N/A
CMD18	N/A	ODT
CMD5	RST	RST



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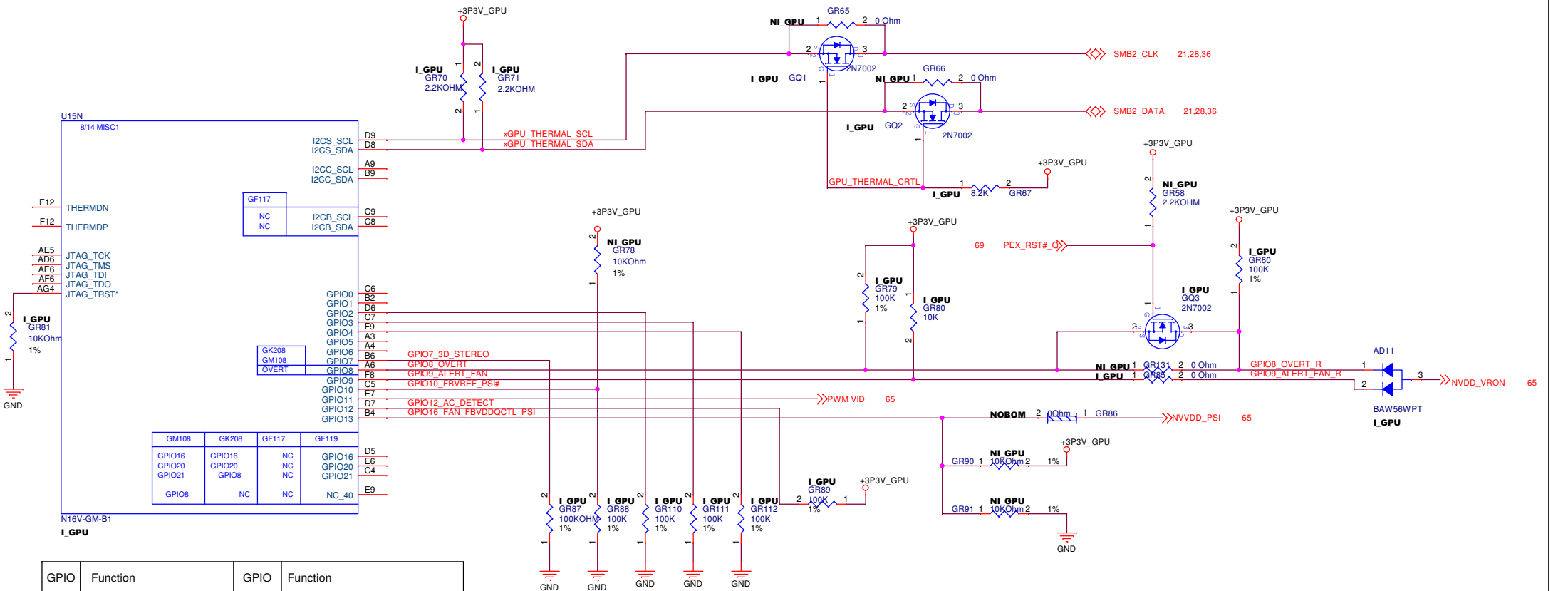
PEGATRON THERMAL Memory Lower A

PEGATRON CORPORATION Engineer: CK_Lee

Size A3 Project Name IPMBW-BR Rev R1.03

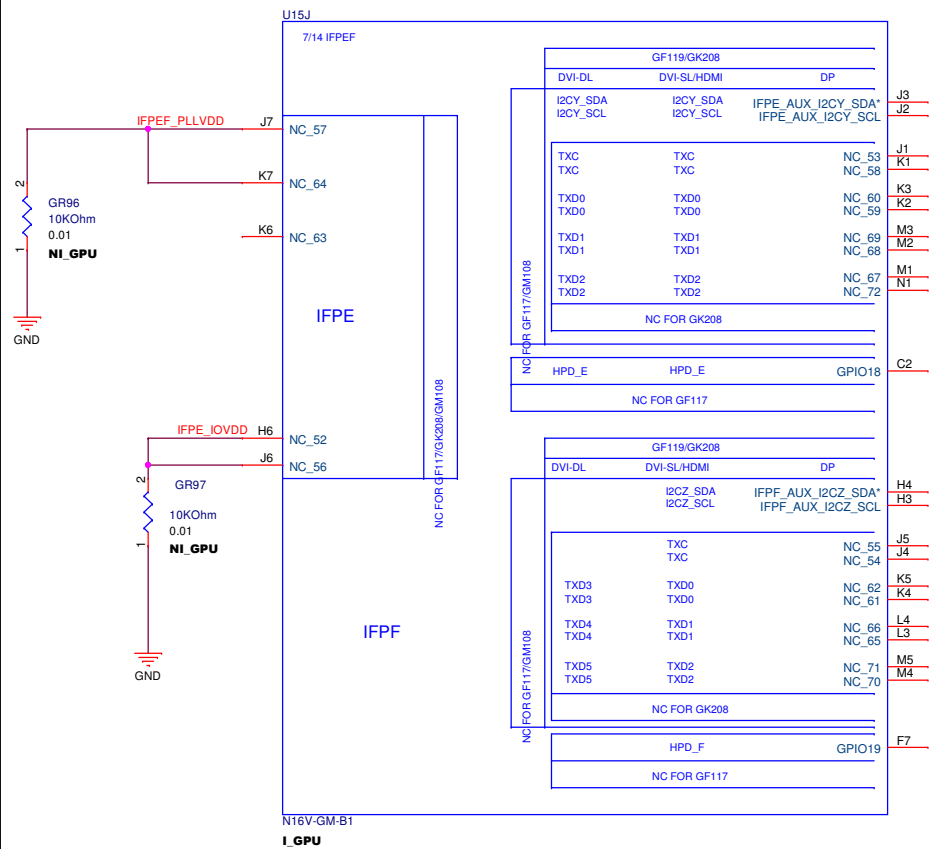
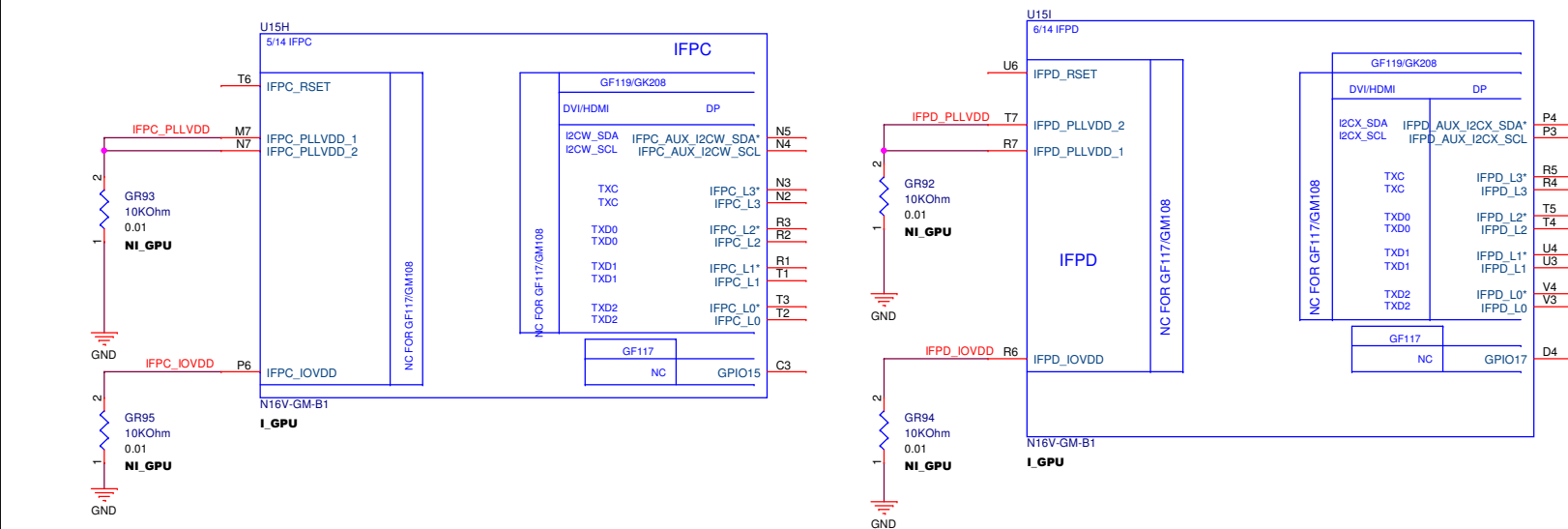
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GPIOs, Thermal Sensor, I2C/GPIO Expanders

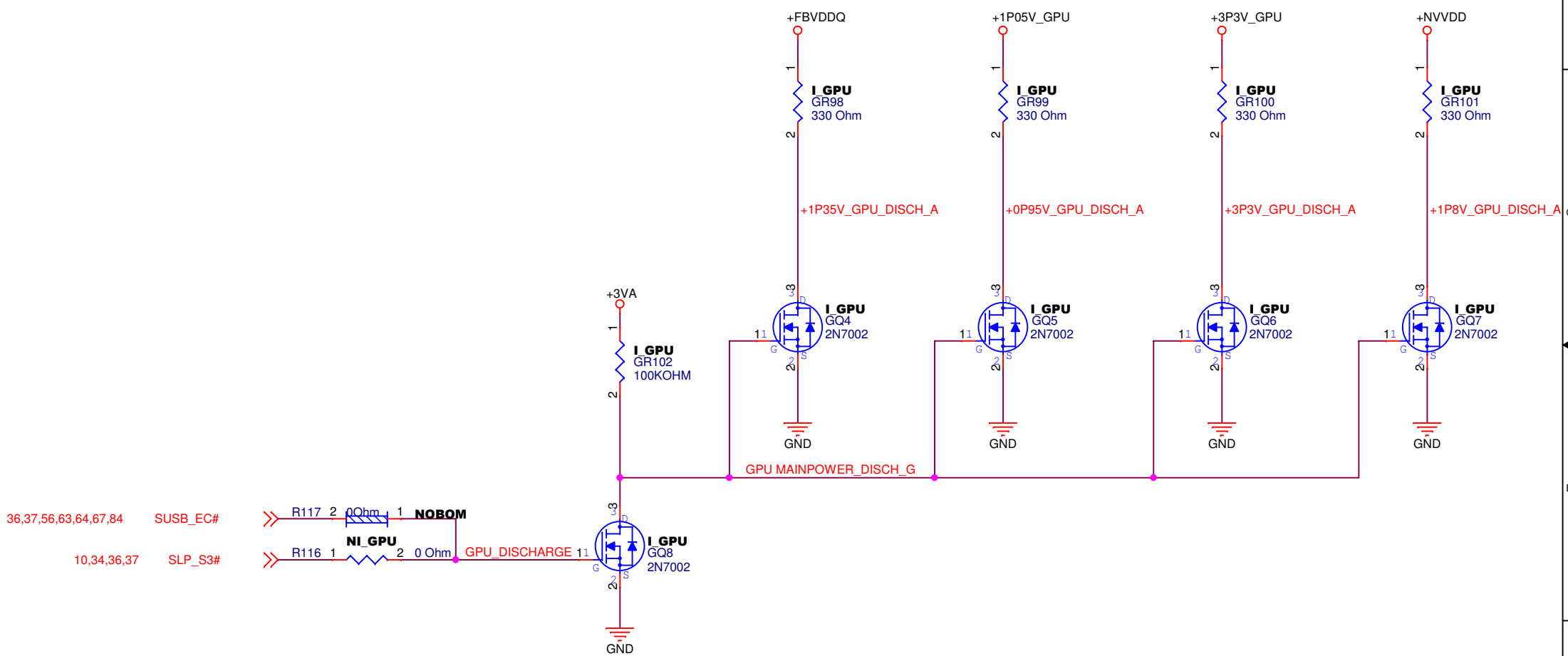


GPIO	Function	GPIO	Function
GPIO 0	Debug/Service Header/Alt_Fan PWM	I2C PORT C	
GPIO 1	VID 2	EXPND 0	Level Shifter Error Correction
GPIO 2	LCD brightness control (BL PWM)	EXPND 1	NVGEM GPIO EXP1/ PS_Margin*
GPIO 3	LCD Power enable (PPEN)	EXPND 2	NVGEM GPIO EXP2/PS_MR*
GPIO 4	LCD Backlight enable (BLEN)	EXPND 3	GPIO_DEBUG_SERVICE HEADER
GPIO 5	VID 0		
GPIO 6	VID 1		
GPIO 7	3D STEREO	EXPND 4	GPU_PS_EN
GPIO 8	GPU Overtemp	EXPND 5	RSVD
GPIO 9	GPU thermal Alert	EXPND 6	PEX_RST
GPIO 10	FB Vref Control (not used sDDR3)	EXPND 7	RSVD
GPIO 11	FBVDD/Q VID (Reserved)		
GPIO 12	PWR_Level AC Detect		
GPIO 13	PS1 Vprgm Enable		
GPIO 14	HPD for IFP AB (not used)		
GPIO 15	HPD for IFP C (HDMI/DP)		
GPIO 16	Fan PWM control		
GPIO 17	HPD for IFP D (DP)		
GPIO 18	HPD for IFP E (DVI-I DL)		
GPIO 19	HPD for IFP F (not used)		
GPIO 20	NVGEM Debug GPIO13		
GPIO 21	NVGEM Debug GPIO14		

IFPD DUAL MODE DP HDMI DVI



GPU POWER DISCHARGE



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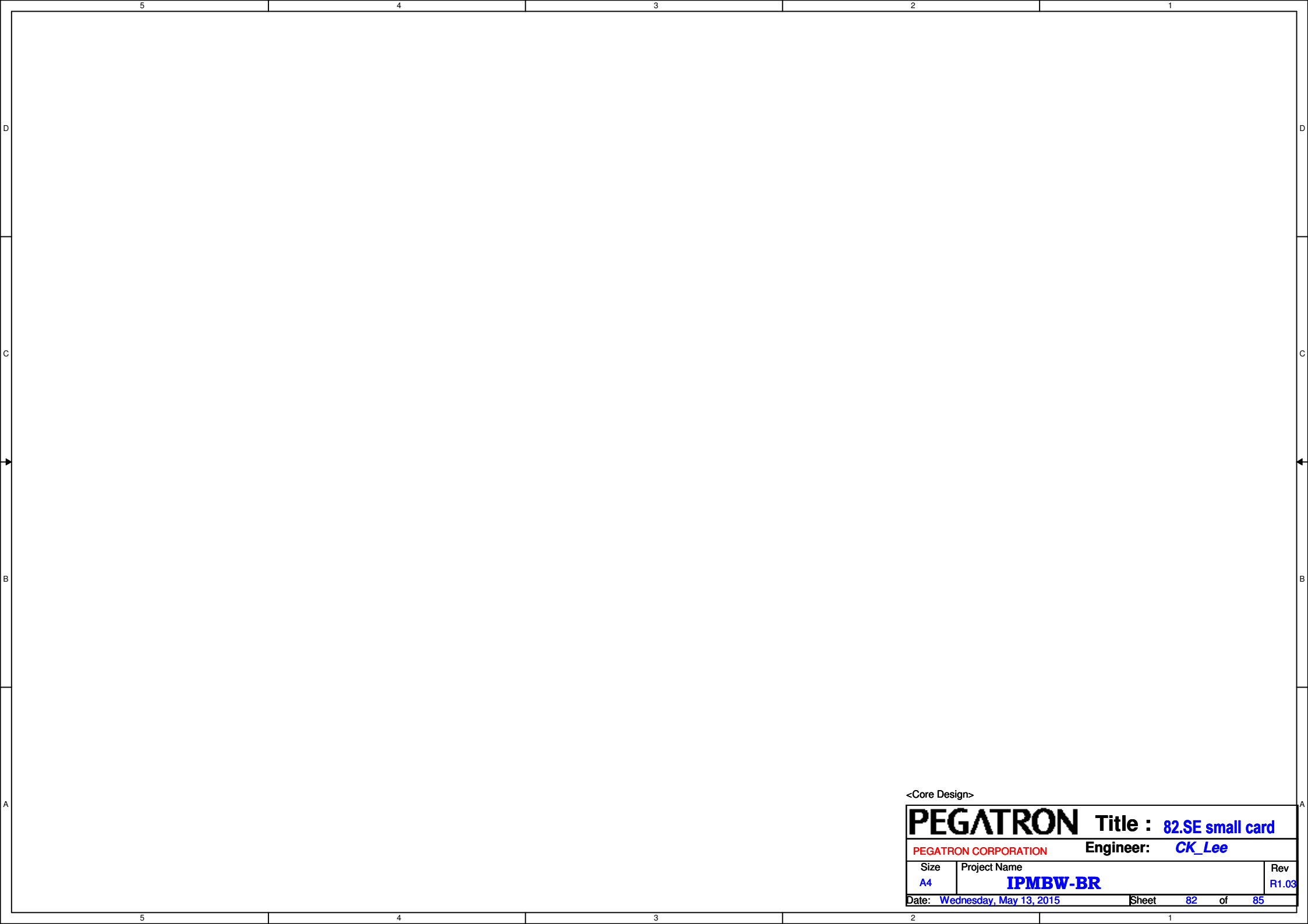
Title : 81.GPU POWER DISCH

PEGATRON CORPORATION

Engineer: CK_Lee

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A4	IPMBW-BR	R1.03

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PEGATRON

Title : 82.SE small card

PEGATRON CORPORATION

Engineer: CK_Lee

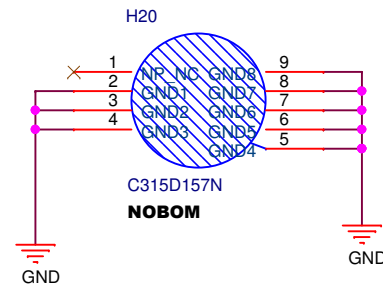
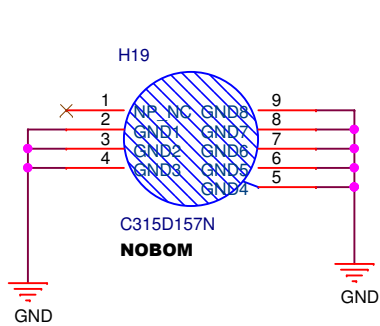
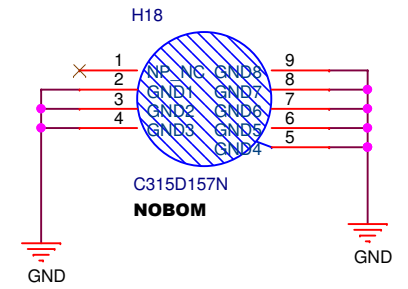
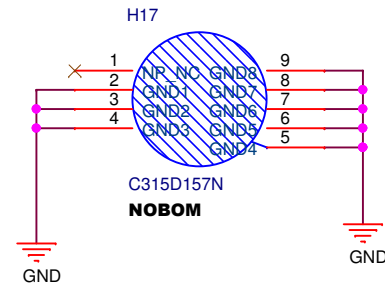
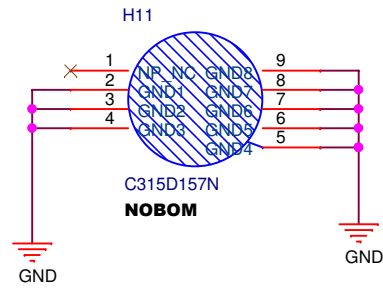
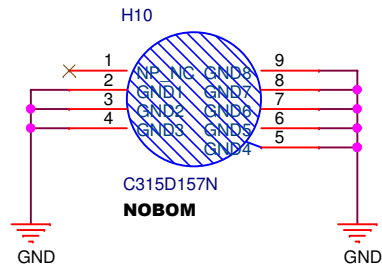
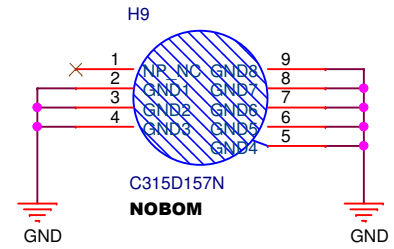
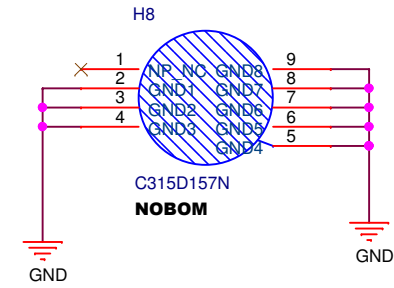
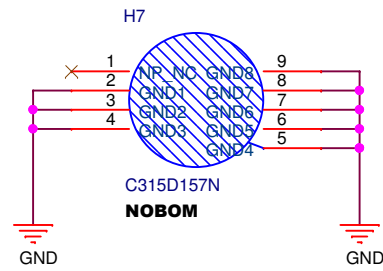
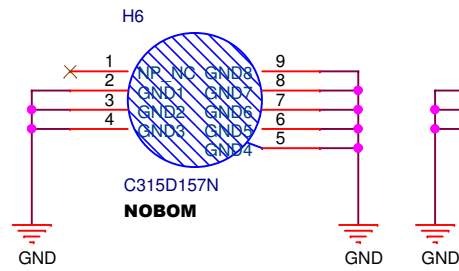
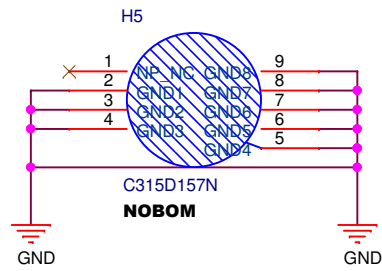
Size
A4

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IPMBW-BR

Rev
R1.03

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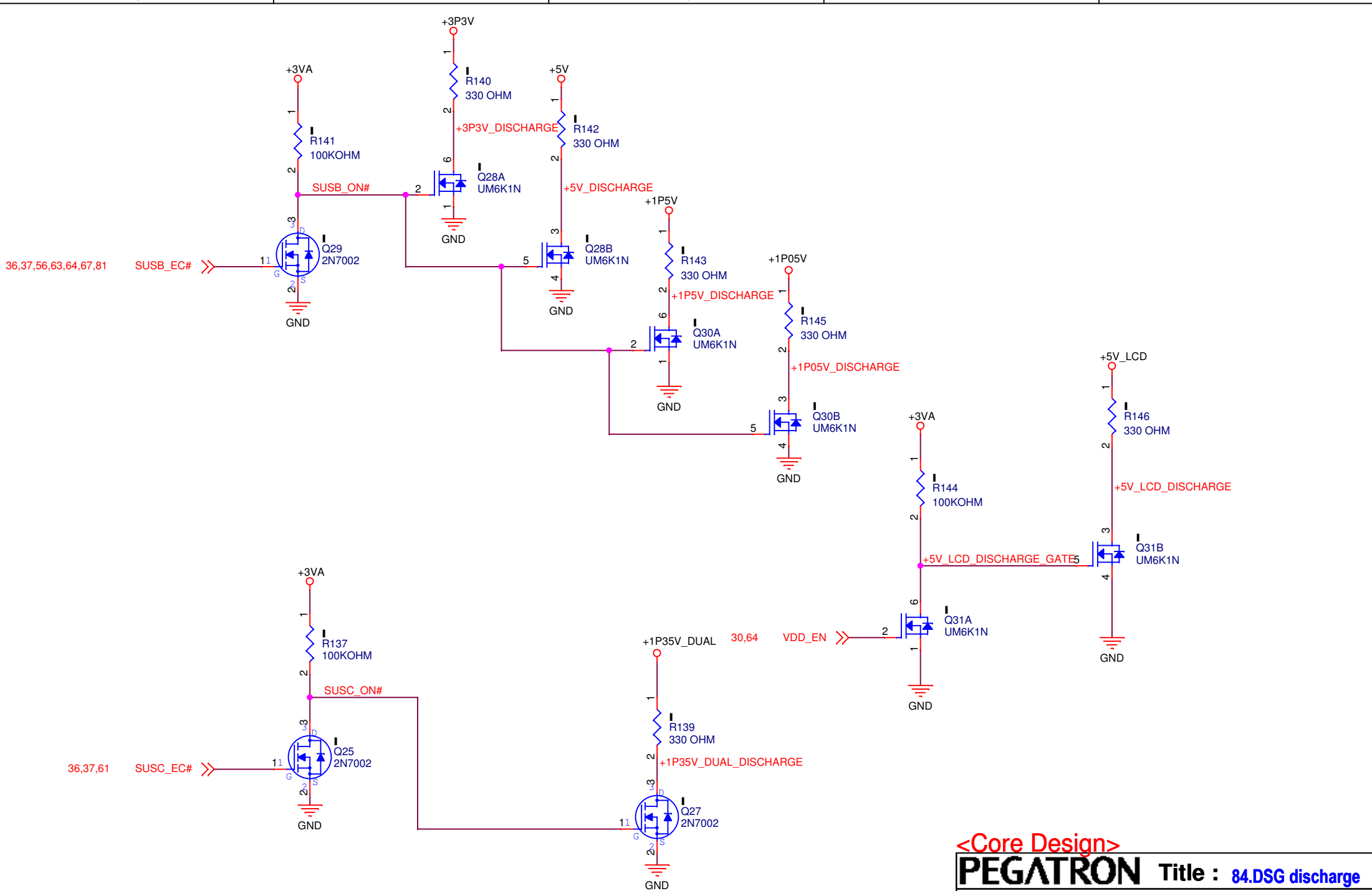
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PEGATRON Title : 83.Screw hole

PEGATRON CORPORATION Engineer: CK_Lee

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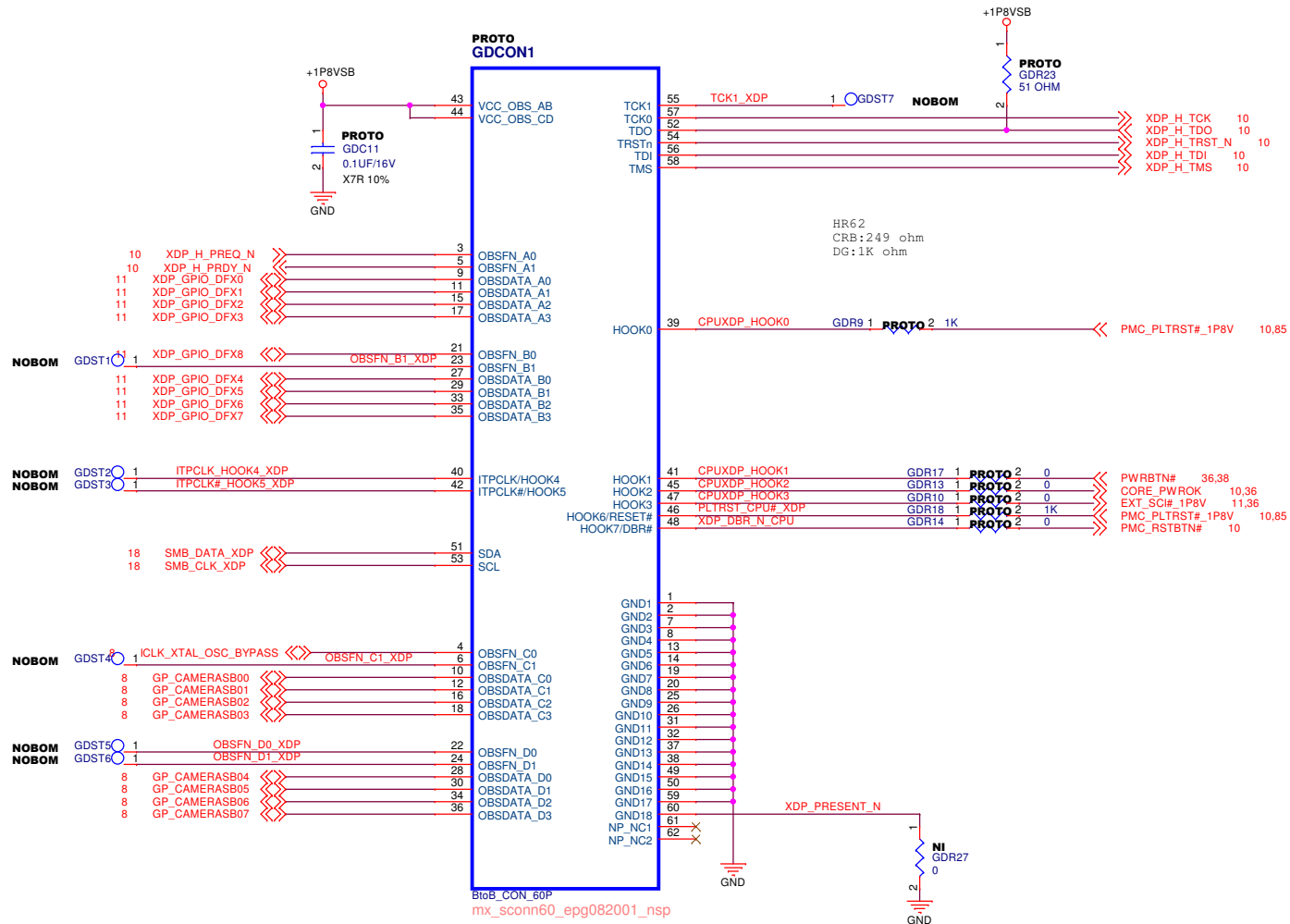
02

1 2 59 60

BOTTOM SIDE VIEW

HRSDF9C-31S-1V(22)^{3W}

PCB FOOTPRINT



PEGATRON		Title : 85.CPU XDP	
PEGATRON CORPORATION		Engineer: CK_Lee	
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